SSA-DM12

Single axis MEMS accelerometer

1. Technical parameter SSA-DM12

Table 1. Technical characteristics SSA-DM12

Parameter	A	B	C	D	Unit
Range	30	50	100	200	g
Bandwidth	100				Hz
Bias stability 10 s averaged 1σ	<50	<100	<200	<300	ug
Bias repeatability by month	300	500	1000	1500	ug
Bias temperature coefficient	<30	<50	<100	<200	ug/℃
Bias temperature hysteresis	<3	<5	<7	<10	mg
SF non-linearity	<1000	<2000	<3000	<3000	ppm
SF repeatability by month	<300				ppm
SF temperature coefficient	10				ppm/℃
Second-order nonlinear coefficient	<100	<100	<50	<50	ug/g^2
Scale factor	250 000	160 000	80 000	40 000	LSB/g
Start-up time	<1				S
Output frequency	2000				Hz
Shock (power on)	10000				g
Shock (power off)	10000				g
Vibration rectification error (6 g RMS)	<0.5	<0.4	<0.15	<0.05	mg/g_{RMS}
Temperature Range	-45 ~ 85				℃
Operating Voltage	5±0.25				V
Current	<10				mA

2. Package Information

2.1 20-pins ceramic package

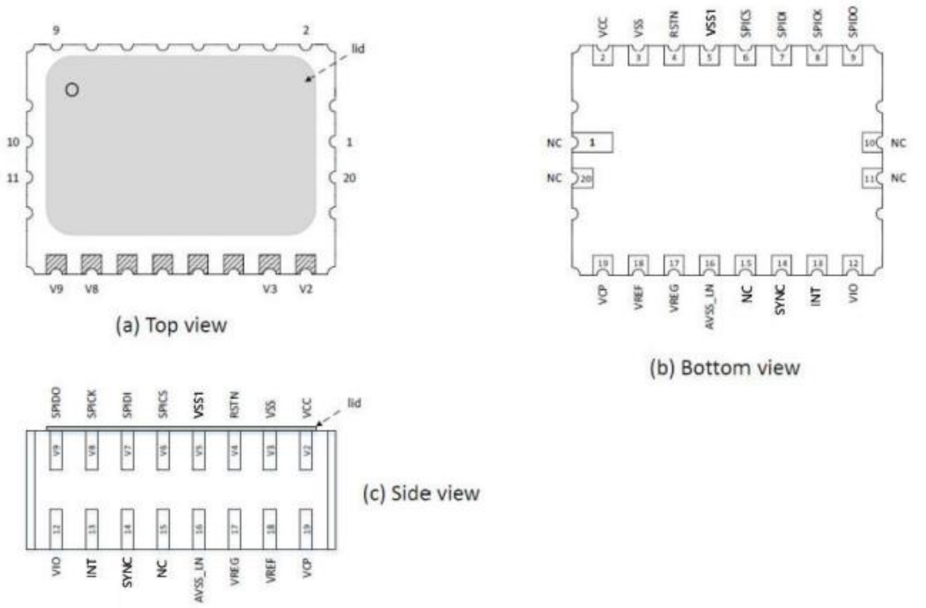

Figure 1. Pin definition of SSA-DM12

Table 2. Pin definition

No	Pin Name	Electric characteristics	Voltage	Description
3,5,V3,V5	VSS	Power ground	0V	
2, V2	VCC	Power input	5V	Power supply voltage requires 0.1uF bypass capacitor to GND
12	VIO	Interface voltage	1.6V~3.6V	The input voltage will be used as the reference voltage of the interface and shall be consistent with the interface voltage of the controller. 0.1uF bypass capacitor is required to GND
6, V6	SPICS	Input	VIO	SPI select
7, V7	SPIDI	Input	VIO	SPI input4
8, V8	SPICK	Input	VIO	SPI clock
9, V9	SPIDO	Output	VIO	SPI output
4, V4	RSTN	Input	VCC	Reset pin, low voltage is activated
17	Vreg	Reference voltage	4 V	Inertial voltage reference, connected to 1 uF bypass capacitor to GND
18	V_{REF}	Reference voltage	2.4 V	Inertial voltage reference, connected to 1uF and 0.1 uF bypass capacitor to GND

Table 2. Pin definition (Continued)

No	Pin Name	Electric characteristics	Voltage	Description
19	VCP	Reference voltage	11V	Inertial voltage reference, connected to 1uF (withstand voltage higher than 16V) bypass capacitor to GND
14	Sync	Input	VIO	Sampling synchronization signal input, can be not connected when not in use
16	AVSS_LN	Internal power	0V	
15,1,10,11, 20	NC			

2.2 Mechanical dimension

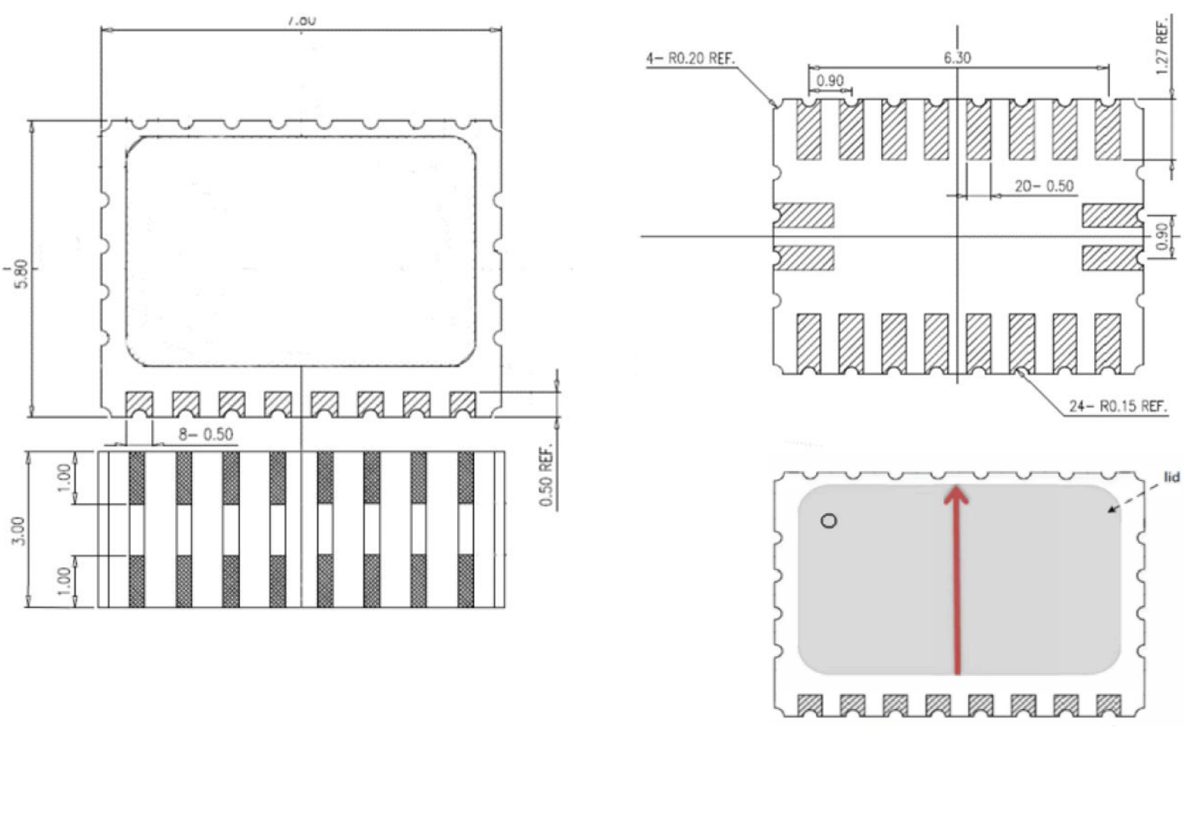

Figure 2. Package information

3. Reference Schematic

3.1 Schematic design

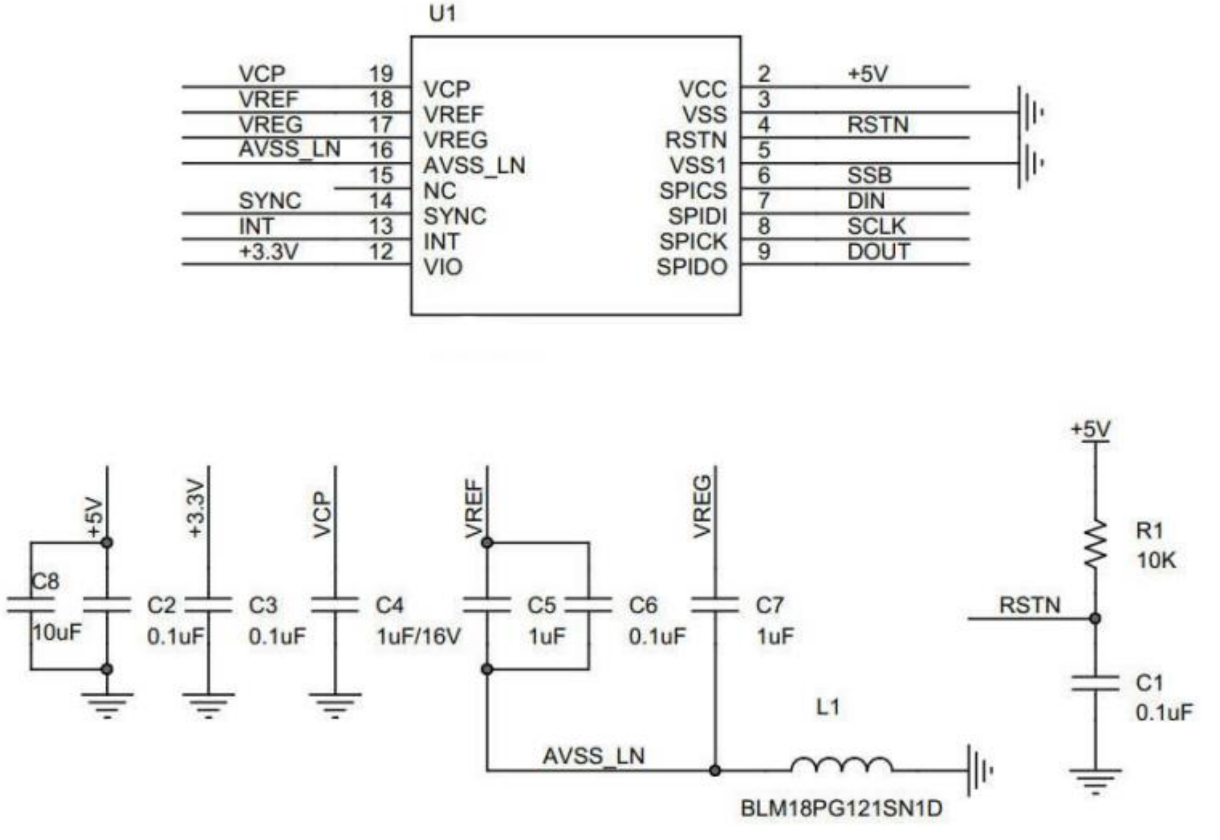

Figure 3. Reference schematic diagram

3.2 PCB Design

1. The decoupling capacitors of pin VCP, VREF and VREG should be placed as close to the pin as possible, and the equivalent resistance of the wiring should be reduced as much as possible.
2. The other end of the decoupling capacitor of VREF and VREG connected to AVSS_ LN as close as possible, and then connected to the GND through magnetic beads.
3. The decoupling capacitance of VCC and VIO should also be placed close to the corresponding pin. The overall current of VCC will be about 10mA. Wide PCB wiring is required to ensure the voltage is stable.
4. To make the device placed horizontally, try to avoid wiring under the package.
5. When arranging the device location, try to avoid the stress concentration area. Avoid large cooling elements, areas with external mechanical contact, extrusion and pulling, and areas prone to warpage during overall installation, such as set screws

4 Communication and Control

4.1 Hardware Interface

4.1.1 SPI interface Timing

SSA-DM12 output data is achieved by reading the specified registers' address. Similarly, the control of SSA-DM12 is realized by writing the value to the specified register. SSA-DM12 registers' writes or reads the specified register address through the 4-wire SPI hardware interface. The SPI interface of SSA-DM12 use the mode 3 timing type in slave mode. That is, CPOL=1, CPHA=1. Before CS is pulled to low voltage, the default voltage of clock is high, and the data is read on the rising edge.

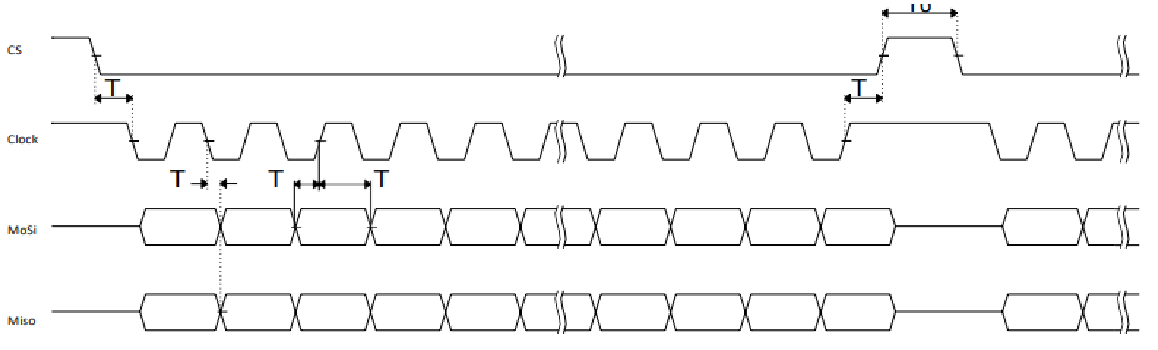

Figure 4. SPI timing parameters

Table 3. SPI timing parameters

Symbol	Parameter	Condition	Minimum Value	Typical Value	Maximum	Unit
Fsclk	SPI clock frequency	DIN/DOUT max load 20 pF		4	8	MHz
T1	Chip selected to clock edge		200			ns
T2	DOUT effective time, after SCLK edge		20			ns
T3	Setup time of DIN, before the rising edge of SCLK		10			ns
T4	The hold time of DIN, after the rising edge of SCLK		10			ns
TDR, TDF	The rise time and fall time of DOUT, not shown in the figure	Vio 3.3 V		10		ns
T5	The high level time of SSB, after SCLK edge		200			ns
T6	Interval between two SPI visits		500			ns

4.1.2 SPI read/write control

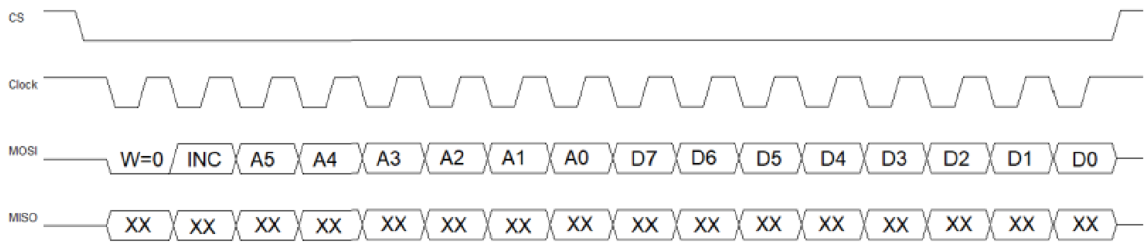

Figure 5. SPI single byte write timing

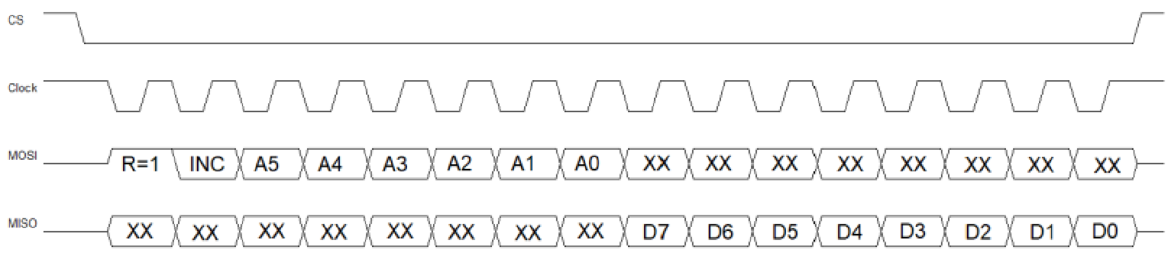

Figure 6. SPI single byte read sequence

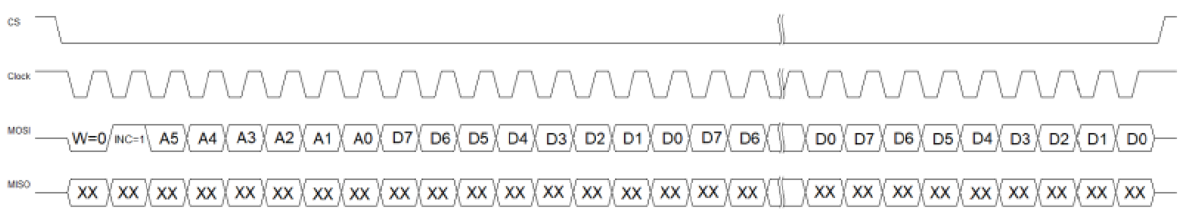

Figure 7. SPI multibyte write timing

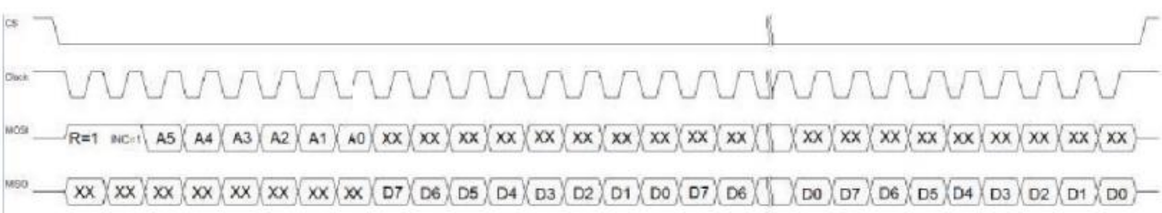

Figure 8. SPI multibyte read sequence

Remarks: W/R: SPI Write/read control byte
0:SPI write
1: SPI read
INC: SPI read and write single byte or multi byte instructions
0:SPI single byte read/write
1: SPI address multibyte read/write
A5~A0: SPI operation address range: 0X00~0X3F
D7~D0: SPI operation data range: 0X00~0XFF

4.2 SPI read/write control

4.2.1 Content of the registers

Register absolute address: 0x19, STATUS

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved							
Output data status flag. Data_Rdy: 1, sensor data if valid; 0, sensor data is invalid							

Register absolute address: 0x1A, TEMP_OUT_L

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Temp_Out [7:0]							
Temperature output, low 8 bits							

Register absolute address: 0x18, TEMP_OUT_H

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Temp_Out [15:8]							
Temperature output, high 8 bits							

Register absolute address: 0x1C, ACC_OUT_L

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ACC_Out [7:0]							
Acceleration output, bit 7:0							

Register absolute address: 0x1D, ACC_OUT_M

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ACC_Out [23:16]							
Acceleration output, bit 23:16							

Register absolute address: 0x1E, ACC_OUT_H

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ACC_Out [23:16]							
Acceleration output, bit 23:16							

Register absolute address: 0x2E, CHIP ID 1

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Chip_ID_1: 0x41							
CHIP_ID_1. Default value: 0x41							

Register absolute address: 0x2F, CHIP ID 2

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Chip_ID_2: 0x01							
CHIP_ID_2. Default value: 0x01							

4 Data format

4.1 Temperature data output

The temperature data is 16bit, two's-complement format, and the highest bit is the sign bit. Register 0X1A (TEMP_OUT_L) is the low byte of temperature output, and register 0X1B (t TEMP_OUT_H) is the high byte of temperature output

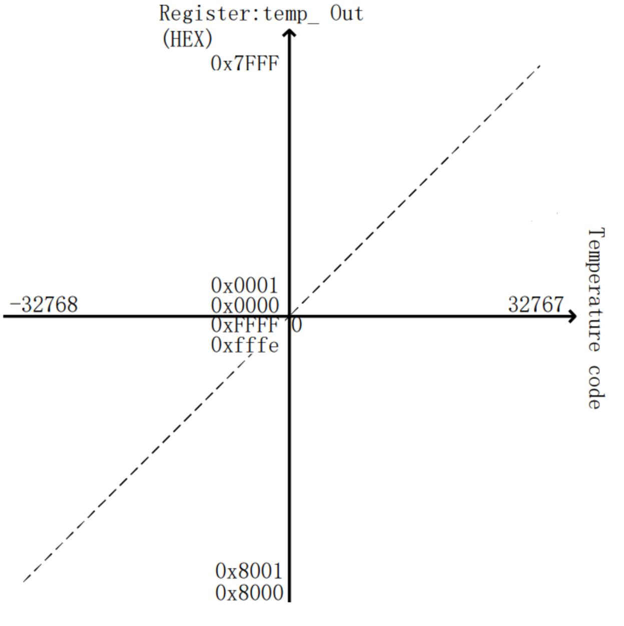

Figure 9.

The corresponding relationship between the temperature output and the actual temperature can be roughly in accordance with the following formula:

$$\text{Actual temperature}(^\circ C) = \frac{\text{Temperature code (DEC)} + 8000}{320} + 22$$

It should be noted that the output of the temperature sensor is usually used as a compensation parameter, so only the relative accuracy is required, and the temperature sensor is inside the chip, and the actual temperature is mainly affected by the temperature self heating. Therefore, the temperature output is not accurately corrected for the Celsius temperature value. The actual Celsius temperature obtained according to the formula can only be used as a rough reference, and the ambient temperature of the environment where the chip is located cannot be measured.

4.2 Temperature data output

The acceleration output is 24bit, two's-complement format, and the highest bit is the sign bit. Register 0X1C (ACC_OUT_L) is the low byte of acceleration output, register 0X1D (ACC_OUT_M) is the middle byte of acceleration output, and register 0X1E (ACC_OUT_H) is the high byte of acceleration output

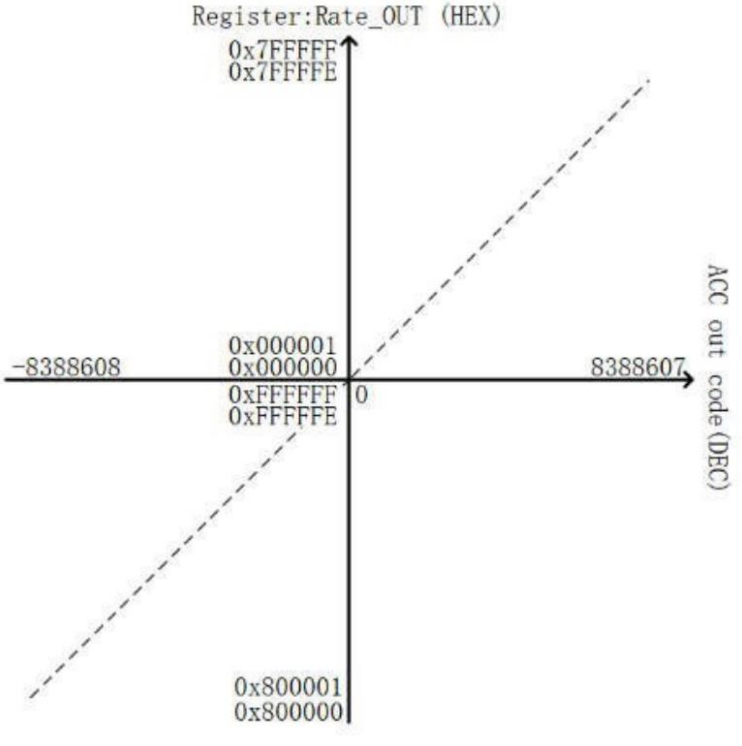

Figure 10.

The corresponding relationship between the value of the acceleration output and the actual acceleration can be as follows:

$$\text{Actual temperature}(g) = \frac{\text{ACC out code (DEC)}}{\text{Scale factor}}$$

Because the product can be customized. In the formula, the scale factor needs to refer to the quality inspection report, when the product is delivered.

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