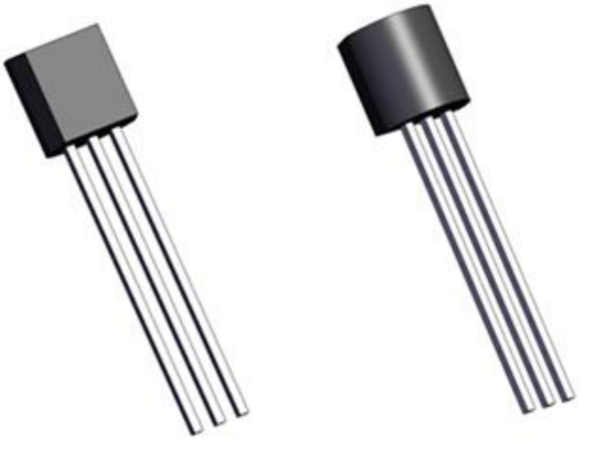
SST-DM11

Programmable resolution 1-wire digital thermometer



PRODUCTS FEATURES

- Operating voltage: 3.0 V – 5.5 V
- Operating current: 38uA during temperature conversion
- Average consumption current: 1.5uA with reading once temperature per second
- Standby current: 100nA, 1000nA
- Temperature conversion time: 30ms at 9-bit
- Temperature accuracy without calibration: ± 0.5 °C. From -10°C to 80°C
- 9 bit ADC for 0.5°C resolution
- Compatible with 1-wire interface
- Temperature range: -50°C to 125°C
- Package: TO-92

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1. Electrical characteristics

Test conditions: Vcc = 3.3V to 5.0V, T_A = 25°C unless otherwise specified. All limits are 100% tested at T_A = 25°C

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Voltage	V_{CC}		3.0		5.5	V
Temperature Accuracy	T_{AC}	VCC = 3.3-5.0V, T_A=-10°C to 80°C	-0.5		0.5	°C
		VCC = 3.0-5.5V, T_A=-50°C to 125°C	-1.5		1.5	°C
Temperature Resolution		9-bit ADC		0.5		°C
Operating Current	I_{OC}	during Temperature conversion		38		uA
Average Consumption Current	I_{AC}	Once time T-conversion per second		1.5		uA
Shutdown Current	$I_{SHUTDOWN}$	Idle, not temperature conversion		100	1000	nA
Conversion time	t_{CON}	From active to finish completely		30		ms
Digital Interface						
Logic Input Capacitance	C_{IL}	I/O pin		20		pF
Logic Input High Voltage	V_{IH}	I/O pin	0.7*VCC		VCC	V
Logic Input Low Voltage	V_{IL}	I/O pin	0		0.2*VCC	V
Logic Input Current	I_{INL}	I/O pin	-2.0		2.0	uA
Communication Timing						
Single-Wire Communication Clock	T_{CLK}			15		us
Recovery time	t_{REC}		3.0			us
Time slot for "0" or "1"	t_{SLOT}		4*T+ t_{REC}			us
Device Reset Low Time	t_{RESET}			32*T		us
Device Reset High Response Time	t_{PDH}			2*T		us
Device Reset Low Response Time	t_{PDL}			8*T		us
Device Reset Response Sampling Time	t_{HSP}		2*T		10*T	us
Write '0' Low Time'	t_{W0L}		4*T		8*T	us
Write '1' Low Time'	t_{W1L}		2.0		1*T	us
Read bit Low Time	t_{RL}		2.5		1*T	us
Read bit sampling Time	t_{HSR}		t_{RL}		2*T	us

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* Note for electrical characteristics:
1) All devices are 100% production tested at T_A = 25°C, all specifications over such temperature range is guaranteed by design, not productions tested.
2) For copy TH, TL[0X48] operation, the minimum voltage should be ever 4.0V

2. Absolute maximum ratings

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC} to GND	-0.3 to 5.5	V
I/O pin Voltage	V_{IO} to GND	-0.3 to 5.5	V
Operation junction temperature	T_J	-50 to 150	ºC
Storage temperature Range	T_{STG}	-65 to 150	ºC
Lead Temperature (Soldering, 10 Seconds)	T_{LEAD}	260	ºC
ESD MM	ESD_{MM}	600	V
ESD HBM	ESD_{HBM}	6000	V
ESD CDM	ESD_{CDM}	1000	V

Recommended operating conditions

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	3.0 ~ 5.5	V
Ambient Operation Temperature Range	T_A	-50 ~ +125	°C

* Note for absolute maximum ratings:
1) Stresses greater than those listed under "Absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at the "Absolute maximum Ratings" conditions or any other conditions beyond those indicated under "Recommended operating conditions" is not recommended. Exposure to "Absolute Maximum ratings" for extended periods may affect device reliability.
2) Using 2oz dual layer (Top, bottom) FR4 PCB with 4x4mm² cooper as thermal PAD

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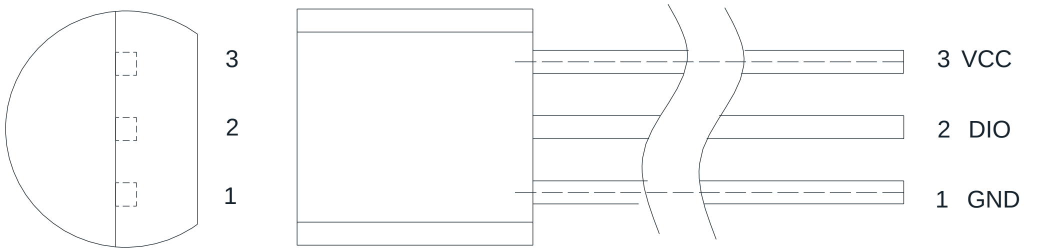
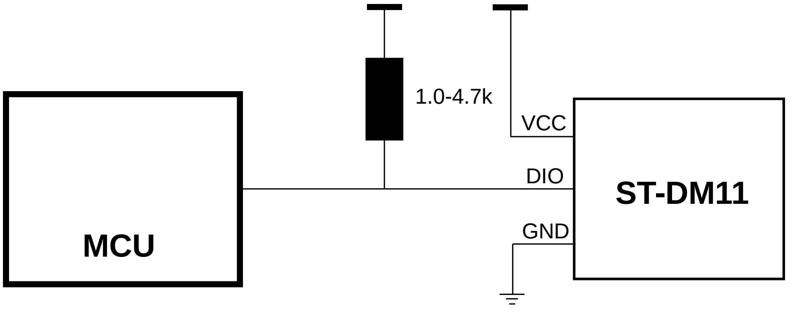
3. Pin configurations



4. Typical application



PIN №	PIN Name	Description
GND	1	Ground pin
DIO	2	Digital interface data input and output pin, generally it needs a pull-up resistor to VCC in most application, between 1.0k and 4.7k
VCC	3	Power supply input pin, it should connect a 100nF to 1.0uF ceramic cap at least to ground

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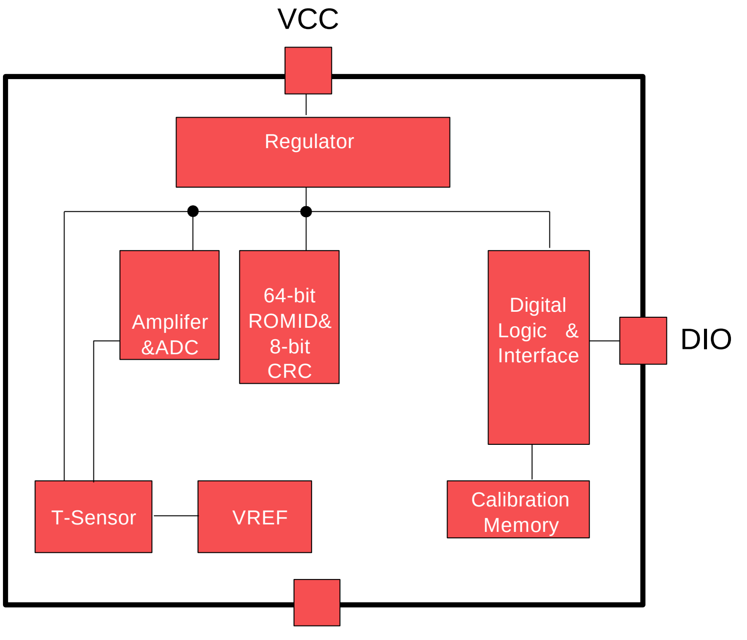
5. Function block



6. Protocol operating diagram

Part 1	Part 2	Part 3
Reset	ROM Function Command and/or Device Function Command	Data Tx/Rx
1. Device Reset Pull-low I/O pin with 450us to 650 us duration	1. ROM Function command, including : 1) Read ROM……0x33 2) Match ROM……0x55 3) Search ROM……0xF0 4) Skip ROM……0xCC 5) Search Temperature Alarm ROM ID…… 0xEC 2. Device function command, including: 1) Write Register……0x4E 2) Read Register……0xBE 3) Temperature conversion……0x44 4) Read power Mode……0xB4 5) Recall TH, TL from memory……0xB8 6) Copy TH, TL register……0x48	Including 1. Read data from the chip, or 2. Write data into register

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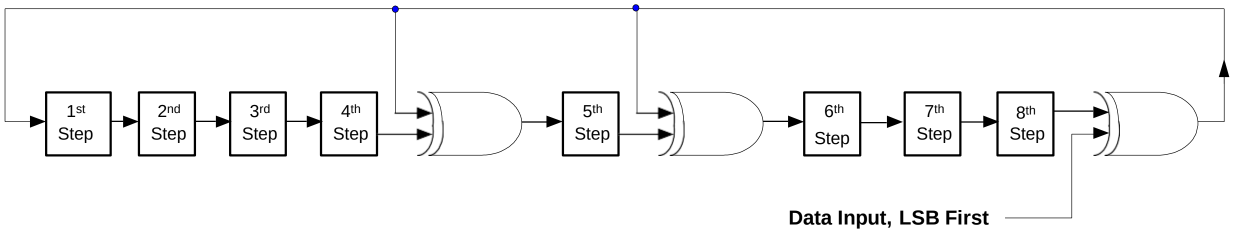
64-bit ROM ID Definition

8 bits	48 bits	8 bits
CRC Code [$X^8+X^5+X^4+1$]	Serial number [48-bit, factory trimmed]	Family code [0x28]
MSB LSB	MSB LSB	MSB LSB

8-bit CRC Code generator diagram



Register map

Byte Address	*Attribution	Register definition		Default value
		Name	Description	
0x00	R/O	TLSB	Temperature data, LSB Byte	0xAA
0x01	R/O	TMSB	Temperature data, MSB Byte	0x00
0x02	R/W	TH	Upper Alarm trigger temperature	0xFF
0x03	R/W	TL	Lower Alarm trigger temperature	0XFF
0x04	R/W	CONFIG	*Configuration register	0X7F
0x05	R/O	Reserved	Reserved Byte 0	N/A
0x06	R/O	Reserved	Reserved Byte 1	N/A
0x07	R/O	Reserved	Reserved byte 2	N/A
0x08	R/O	CRC	CRC code byte (8-bit)	N/A

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*Note:

1. These registers data can be changed by writing Register command, after power on reset, the data will reload from memory.
2. In Attribution column, R/O means read only; R/W means readable/writable
3. For CONFIG register, all R/W bits are reserved for testing, DO NOT write any data into these bits.

7. Function descriptions

The chip can sense temperature and convert it into digital data by a 9-bit ADC. Also the chip supports user-programmable upper/lower trigger temperature settings. Single-Wire interface is compatible with 1-wire and the protocol shown in Figure-3. Generally, one complete communication with host, like MCU, should include Part1, Part2 and Part3. For Search ROM, it is an exception. The device supports 5 ROM function commands and 6 Device Function commands. First, the host issues above ROM function commands; then after successful completion, the chip can be accessed via above Device function commands by the host. SST-DM11 can be powered by the local power supply; it can also be powered from the communication line, which is called parasitic power supply. It is recommended to force power supply pin at VCC pin for high precision temperature application. The chip has 8 registers; the register address is from 0x00 to ox07. And each register has 8-bits, 1-byte. The last byte, 9th-byte is CRC code generated by above 8 bytes register data. The detail information is shown in “Register map”. All registers data can be read out by read register command, 0xBE. TH, TL and CONFIG register can be written by write register command, 0x4E

7.1 Temperature Data [Byte Add: 0x00, 0x01]

The major function of the chip is to measure temperature. The A-to-D converter resolution of the sensor is 9 bit, corresponding to 0.5°C. The SST-DM11 powers up in a low-power idle state. To initiate a temperature measurement and A-to-D conversion, the host has to issue a Temperature Conversion command [0x44h]. After the conversion, the temperature data is stored in the 2-byte temperature register, TLSB [0x00] and TMSB [0x01], and then the chip returns to idle state. The temperature data is stored in the temperature register as a 9-bit sign- extended two’s complement format in degrees Celsius. It is composed by 8 'S' bits (signature) and 8 'DATA' bits. The signature bits(S) indicate if the temperature is positive or negative: for positive numbers S = 0 and for negative numbers S = 1. The 'DATA' bits express the temperature in Celsius degree directly, and the resolution is 0.5°C, and the expressed range is from -127°C to +127°C.

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The maximum operation temperature range of the chip is -50°C to +125°C, since the chip is based on semiconductor process and material. The default temperature data is 85°C after power-on reset. Below tables show the examples of digital output data and the corresponding temperature (°C).

16-bit temperature data format [MSB, LSB]

Temperature (°C)	16-bit Digital Output (HEX)	16-bit Digital Output (BIN)
+127.5	0x00FF	0000, 0000, 1111, 1111
+125.0	0x00FA	0000, 0000, 1111, 1010
+85.5	0x00AB	0000, 0000, 1010, 1011
+25.0	0x0032	0000, 0000, 0011, 0010
+10.5	0x0015	0000, 0000, 0001, 0101
+0.5	0x0001	0000, 0000, 0000, 0001
0.0	0x0000	0000, 0000, 0000, 0000
-0.5	0xFFFF	1111, 1111, 1111, 1111
-10.0	0xFFEC	1111, 1111, 1110, 1100
-25.0	0xFFCE	1111, 1111, 1100, 1110
-50.0	0xFF9C	1111, 1111, 1001, 1100

Temperature data in register

	Byte Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
LSB	0x00	2^6	2^5	2^4	2^3	2^2	2^1	2^0	2^{-1}
Celsius degree[°C]		64	32	16	8	4	2	1	0.5
MSB	0x01	S	S	S	S	S	S	S	S
Celsius degree[°C]		sign	Sign	sign	sign	sign	sign	Sign	sign

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7.2 Temperature Alarm Setup, TH & TL [Byte Add: 0x02, 0x03]

Temperature conversion results will be automatically compared with the temperature alarm value setup by user to determine whether there is an alarm condition. Alarm threshold also uses 2's complement format with 8-bit (1 bit sign, S + 7 bits data). Alarm temperature is set to 1°C increments with 1-byte shown as below table. If the temperature conversion result is greater than or equal to TH value or less than the TL value, it will generate an alarm flag on single-wire bus. After a temperature alarm, the device will respond with a Search Temperature Alarm ROM ID command, 0xEC. If the result of the subsequent temperature conversion value is within the TH and TL defined range, the alarm condition is removed. The TH and TL registers data are stored with nonvolatile Memory, so they will retain data when the device is powered down. Also TH and TL can be accessed and changed using read or write register command. However TH and TL data are loaded from memory every time after power on reset or using recall memory command, 0xB8. For threshold temperature of TH, TL, the format is shown as below table.

Temperature Limit Threshold Bit Definition

	Byte Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TH	0x02	S	2^6	2^5	2^4	2^3	2^2	2^1	2^0
Celsius degree[°C]		sign	64	32	16	8	4	2	1
Default [0x55, 85°C]		0	1	0	1	0	1	0	1
TL	0x03	S	2^6	2^5	2^4	2^3	2^2	2^1	2^0
Celsius degree[°C]		sign	64	32	16	8	4	2	1
Default [0x00, 0°C]		0	0	0	0	0	0	0	0

7.3 Config Register [Byte Add: 0x04]

The chip has a 8-bit (1-Bytes) configuration register, bit0, bit1, bit2 and bit7 are readable/writable attribution for user. All 4 bits is reserved for testing and do not write any data into this register via write register command, 0x4E. Also user can read out register data. And the register will reset to default data after power-up. 8 bits definition is shown as below table.

Config Register definition

Byte Add, 0x04	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Definition	Reserved	N/A	N/A	Reserved	N/A	Reserved	Reserved	Reserved
Attribution	R/W	R/O	R/O	R/O	R/O	R/W	R/W	R/W
Default, 0x7F	0	1	1	1	1	1	1	1

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8. ROM function command

After the host detects a presence pulse, it can issue a ROM function command. These commands are related to each device's unique 64-Bit ROM ID code, allowing multiple Single-Wire devices connected on a single bus line and operated accordingly. These commands also allow the host to detect the number of Single-Wire devices and the types, and whether a device is in the alarm state. Each device supports basic 8 kinds ROM command, each command code length is 8-bit. Before Device Function commands are issued, the host must submit the appropriate ROM Function command. ROM Function command operation flowchart is shown in application note. And there is a brief description for each ROM Function command and the usage.

8.1 Read ROM [0x33]

This ROM command only applies to one device on Single-Wire bus. It allows the host to read directly the device's 64-Bit ROM ID code without performing a search ROM. If the command is used for multi-node connections, data conflict is inevitable because each device will respond to this command at same time.

8.2 Match ROM [0x55]

This command is followed by 64-ROM ID allowing the host to access a specified Single-Wire device in multi-node connections. Only when the slave device completely matches 64-Bit ROM ID, it will respond to the function command that host issued; all other devices will wait for a reset pulse.

8.3 Search ROM [0xF0]

When the system powers up, the host must identify all Single-Wire devices' ROM ID codes on the bus. And therefore the host can determine the number and the type of devices. By repeatedly performing a Search ROM command (Search ROM command followed by bits of data exchange), the host identifies all Single-Wire devices on the bus. If the bus has only one device, you can use the read ROM command to replace Search ROM command. After completion of each ROM search, the host must return to the first step in the command sequence (initialization).

8.4 Skip ROM [0xCC]

In a single-node application, the host can use this command to quickly access the device on the bus without issuing identical ROM ID code information, which saves corresponding time instead of sending the 64-Bit ROM ID. However in a multi-node application, if the host wants all devices on the bus to perform the same subsequent function command, the host can also use the Skip ROM command. For example, the host issues a Skip ROM command before a Temperature Conversion [0x44] command; then all the SST-DM11 devices on the same bus will begin the temperature conversion simultaneously. In this way it saves time for performing the entire temperature measurements and gets the temperature conversion results simultaneously.

This example is particularly useful for the analysis of temperature fields. Please note, if user issue a Skip ROM command followed by a Read Register [0xBE] command (including other read command), this command can only be applied to a single node system; otherwise multiple nodes will respond to the command and therefore cause conflicting communication data.

8.4.1 Search Temperature Alarm ROM ID [0xEC]

Only those Single-Wire devices with temperature alarm flag respond to this command. This works exactly the same as the search ROM ID command. This command allows the host to determine which device has generated the temperature alarm In the same way as Search ROM ID command, after the completion of the search cycle, the host must return to the first step in the command sequence.

9. Device Function Command

Device Function command is similar as above ROM Function command and the flowchart describes the implementation of several commands and function command protocol such as read/write Register, start temperature conversion, and read/write memory commands. And there are brief description for each Device Function command and the usage.

9.1 Write Register [0x4E]

This command allows the host to write 3-bytes of data into SST-DM11 Register register. The first byte is TH register (byte address 0x02), the second byte the TL register (byte address 0x03), and the third byte the configuration register (byte address 0x04). Data is transmitted starting from the least significant bit. Before the host sends a reset signal, these three bytes must be written, otherwise it may lead to an error of incomplete data transfer.

9.2 Read Register [0xBE]

This command allows the host to read the contents of the Register register. Data transmission always starts from byte address 0 (the least significant bit of the temperature register) and continues until finishing the remaining seven bytes of Register. If the host continues to read, it reads the 9th byte, the 8-Bit CRC. The CRC is generated by SST-DM11 using the same polynomial in ROM ID CRC generator. CRC is sent in the original format. If only part of the register data is needed, the host can send a reset signal to end this reading operation.

9.3 Temperature Conversion [0x44]

This command starts the temperature conversion. After the conversion is complete, the measured temperature data will be stored into the registers (byte address, 0x00, 0x01.). SST-DM11 then returns to a low-power idle state. If the device is in "parasitic power mode", the host pulls Single-Wire bus into the strong state (the time value and resolution independent) after sending the command. The host monitors the conversion process in each time slot. When the host reads the logic '1 'instead of '0', it indicates the temperature conversion is complete.

9.4 Read Power Mode [0xB4]

When this command is executed, the host will receives 0xFF if the chip is power in normal supply mode (force power at VCC pin), or receives 0x00 if the chip is powered in parasitic mode (VCC pin is short to GND, the chip is powered by DIO pin)

9.5 Recall TH, TL [0xB8]

This command will recall the TH and TL alarm values from backup memory, and copy them to the associated registers (Byte add, 0x02 and 0x03). After this command code is sent, the host sends a read time slot to monitor the recall process. When the host reads “1” instead of “0”, it indicates that the data read back is complete. When the chip powers up every time, the register data is automatically loaded from the corresponding memory address as default data.

9.6 Recall TH, TL [0xB8]

This command copies the register contents of the TH and TL registers Data written by issuing Write Register command [0x4E] into Memory. If the chip is used in parasite power mode, within 10μs (max) after this command is issued the host must switch to a strong pull-up condition on the Single-Wire bus for at least 10ms.

10. CRC generator

CRC (Cyclic Redundancy Check) bytes are provided as part of the chip’s 64-bit ROM ID code and in the 9th byte of the register. For the ROM ID code, CRC part is calculated based the first 56 bits and is contained in the most significant byte of the ROM ID code. The register CRC is calculated from the data stored in the Register, and therefore it changes when the data in the Register changes. The CRCs provide the host with a method of data validation when data is read from the chip. To verify that data has been read correctly, the host must do calculation the CRC based on the received data and then compare this value to either the ROM code CRC (for ROM reads) or to the Register CRC (for Register reads). If the calculated CRC matches the read CRC, the data has been received error free. The comparison of CRC values and the decision to continue with an operation are determined entirely by the host. The equivalent polynomial function of the CRC (ROM or Register) is:

CRC = $X^8+X^5+X^4+1$

The host can re-calculate the CRC and compare it to the CRC values from the SST-DM11 using the polynomial generator shown in the section “8-bit CRC Code generator diagram”. This circuit consists of a shift register and XOR gates, and the shift register bits are initialized to 0x00. Starting with the least significant bit of the ROM ID code or the least significant bit of byte 0x00 in the Register, one bit at a time should shifted into the shift register. After shifting in the 56th bit from the ROM or the most significant bit of byte 7 from the Register, the polynomial generator will contain the re-calculated CRC. Next, the 8-bit ROM code or Register CRC from the SST-DM11 must be shifted into the circuit. At this point, if the re-calculated CRC was correct, the shift register will contain all 0s. The summarization for the CRC generator is shown as below, which can be used for software reference:

a) Data input with LSB first
b) Polynomial is CRC = $X^8+X^5+X^4+1$
c) Data movement is left shift
d) Initial data always is 0x00
e) Data length is 8-bit

When put CRC data as input the result must be the initial data, 0x00

11. 64-bits ROM ID

Each SST-DM11 contains a unique ROM ID code as serial number. First 8 bits are Single-Wire family code, for this chip, it is 0x28, the next 48 bits are unique serial number, the last 8 bits is the CRC code generated based on previous 56 bits, shown in section “64-bit ROM ID Definition”. The shift register is first initialized to 0, then shifts the family code; each time shifted one bit, least significant bit first,. After the 8th bit of family code is shifted, it starts to shift 48 bits serial number. After the last bit of serial number is shifted, the shift register contains the CRC value. After shifting the 8-Bit CRC, all the bits of the shift register are same as initial data, 0x00.

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12. Single-Wire bus

Single-Wire bus system consists of a host and one or more salve devices. In any case, SST-DM11 are slave devices. The bus host could be a microcontroller or SoC. Discussion of Single-Wire bus system is divided into three parts: the hardware configuration, the operation sequence and Single-Wire timing.

12.1 Hardware Configuration

According to the definition of Single-Wire bus system, it has only one data line physically. In order to facilitate this, each device on the bus needs to have open-drain or tri-state output, and SST-DM11's Single-Wire port (DIO pin) uses an open-drain output. A typical circuit is shown in the section “Typical application”. Multi-node system consists of a Single-Wire host and multiple slave devices. SST-DM11 supports around 16kbps (default rate) of fixed and variable communication rate. Pull-up resistor depends primarily on the number of nodes, the communication distance and the line load. For example with the communication distance of less than 20cm, a single node and an independent power supply condition, SST-DM11 requires an external 4.7kΩ (typical) pull-up resistor. If the communication distance is greater than 30m, you need a 1.0k or smaller pull-up resistor even with single-node and an independent power supply, Single-Wire bus idle state is high. If for some reason the device needs suspend temporally and then return to work, it must be placed on the bus idle state.

12.2 Operation Sequence

To access this sensor chip through Single-Wire port, the complete procedure is shown in the section “Protocol operating diagram”, it includes:

Part 1: Device Reset, refer to below section for description in detail.

Part 2: bus function command, including ROM Function command and Device Function command. In most cases, Device Function command is followed by ROM Function command. Sometimes, ROM Function
command can be used independently without Device Function command, like Search ROM.

Part3: Data Receiving/Transmitting, includes receive data from Single-Wire device or send data to Singe- Wire device.

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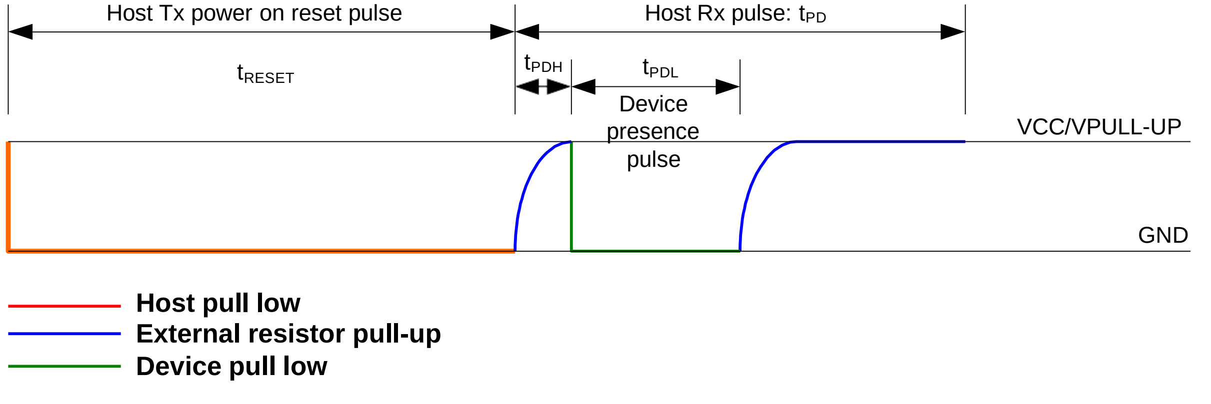
12.3 Device Reset

When the chip is applied power first time, it will perform internal Device Reset action automatically, reset all registers and configurations as initial state, and recall memory data into register as default. All operations of Single-Wire bus always begin with a Device Reset. Device Reset consists of a reset pulse sent by the host and a device responses pulse shown in below “Device Reset Timing Diagram”. The presence pulse is used to notify the host that the chip is already connected on the bus. When a Single-Wire device sends a response pulse to the host, it tells the host that it is on the bus and ready to work. During the initialization process, host pulls the bus low for t_{RESET} period time, thus produces (Tx) Device Reset pulse. Then, the host releases the bus and goes into receive mode (Rx). When the bus is released, the bus is pulled up by an external pull-up resistor. When a Single-Wire device detects a rising edge, it will remain high for t_{PDH} (2T in typical), then the Single-Wire device generates a presence pulse by pulling the bus low for t_{PDL} (8T in typical). After that the bus is released and pulled back high by the external pull-up resistor, at least keeping the 6T time. Thus, the entire Single-Wire device response cycle is at least t_{PD} (16T in typical). After that, the host can begin to transfer the ROM command. If user needs more precise communication time match, the host can measure the Single-Wire device response t_{PDL} (8T in typical) low pulse, and adjust the time of the original Device Reset pulse, t_{RESET}, and the read sampling timing. Once the device successfully captures the communicate reset pulse, it will use it to set the communication speed.

Device Reset Timing Diagram



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12.4.1 Single-Wire Timing

After complete reset successfully on Single-Wire bus, the next step is to perform ROM Function command and/or Device Function command. The following section is to descript the bit transmission. All Single-Wire devices require to strictly comply with Single-Wire communication protocol to ensure data integrity. The protocol defines several signal types: power-on reset pulse, communications reset pulse, presence pulse, write “0”, write “1”, read “0”, and read “1”. All these signals except presence pulse are synchronous signals issued by the host. And all the commands and data are the low byte first which is different from other serial communication format (high byte first).

During Write Time Slot the host writes data to a Single-Wire device; and during the Read Time Slot, the host reads the data from the Single-Wire device. In each time slot, the bus can only transmit one bit data.

12.4.2 Write Time Slot

There are two write time slot modes: write "1" and write "0" slot. The host writes into Single-Wire device "1" by using a write "1" slot, and host write into Single-Wire device "0" by using write "0". All write time slots are at least t_{SLOT} (4*T + t_{REC} in typical), and need the recovery time at least 3μs between two separate time slots. Two kinds of write slots start with pull-down bus by the host shown in below Figure. To produce a write "1" slot, the host must release the bus within t_{W1L} (<= 1*T) after pulling down for 1us, and then the bus is pulled-up by an external pull-up resistors on the bus. To produce a write "0" slot, after the host is pulling the bus low, it maintains a low level during the entire time slot, that is t_{W0L} (> = 4T). During the write time slots, Single-Wire device samples bus level status at t_{SSR} (2*T in typical) time. If sampling results at this time is high, then the logic "1" is written to the device; If "0", the write logic is "0".

12.4.3 Read Time Slot

Single-Wire device can only transmit data to the host after the host issues read time slots. After the host issues a read data command, a read time slot must be generated in order to read data from the Single-

Wire device. A complete read time slot is at least t_{SLOT} (4*T + t_{REC}), and requires at least 3us recovery time between two separate time slots. Each time slot is generated by the host to initiate the read bit, a low level period is required to be at least 1μs shown in below Figure. Once the device detects a Single-Wire bus low, the device immediately sent bit "0" or "1" on the bus. If Single-Wire device sends "1", the bus is pulled-up

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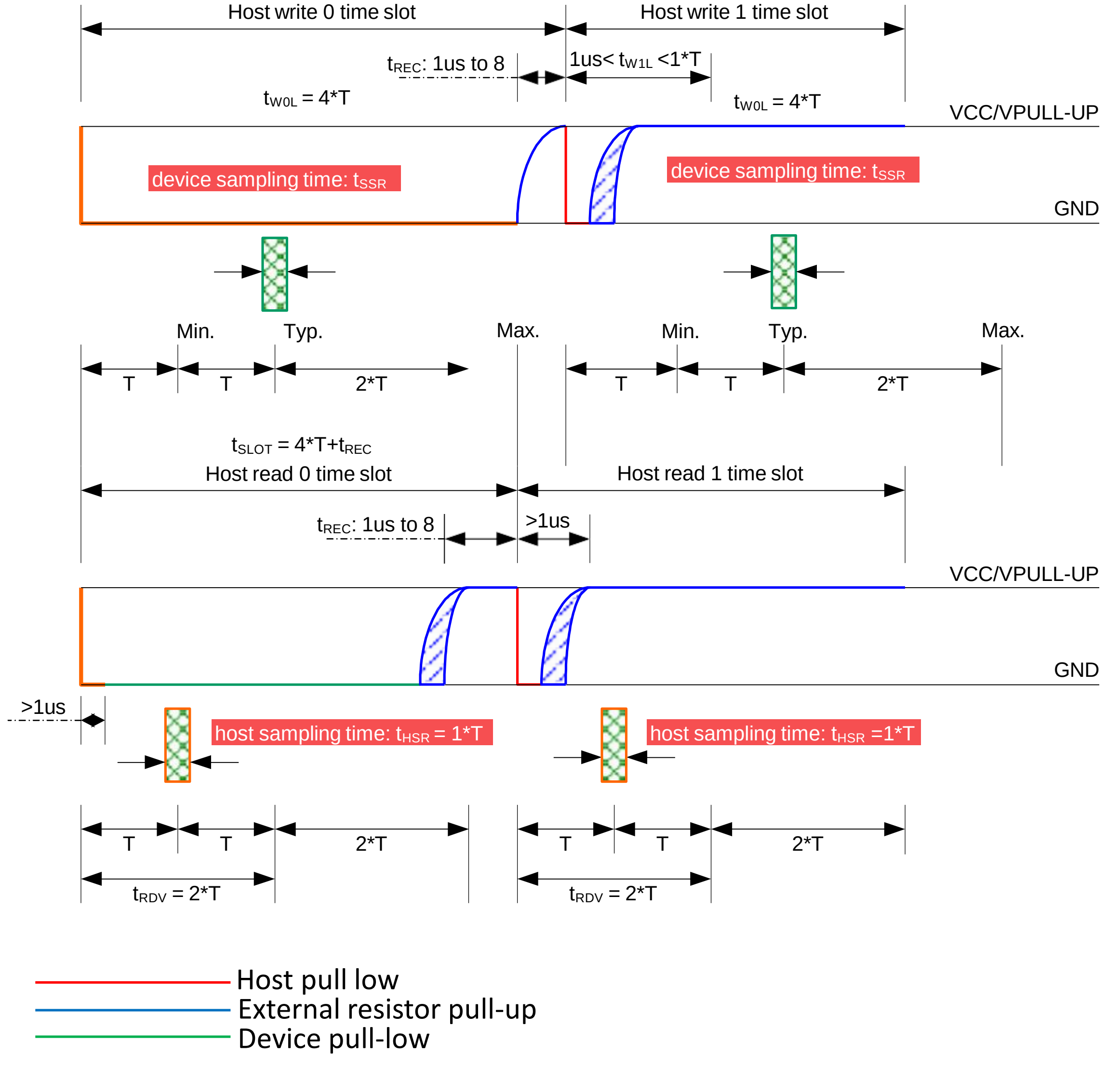
high by a pull-up resistor after the short low period; if sent "0", then the bus is keeping low for t_{DRV} (2*T in typical). After that the device releases the bus from pull-up resistors and back to idle high. Therefore, the data issued by Single-Wire device after read time slot at the beginning stay effective during time t_{DRV} (2*T in typical). During the read time slots the host must release the bus, and samples the bus states at 2T after the start of a slot (optimum sampling time point 1T).

Read/Write Timing Slot Diagram:



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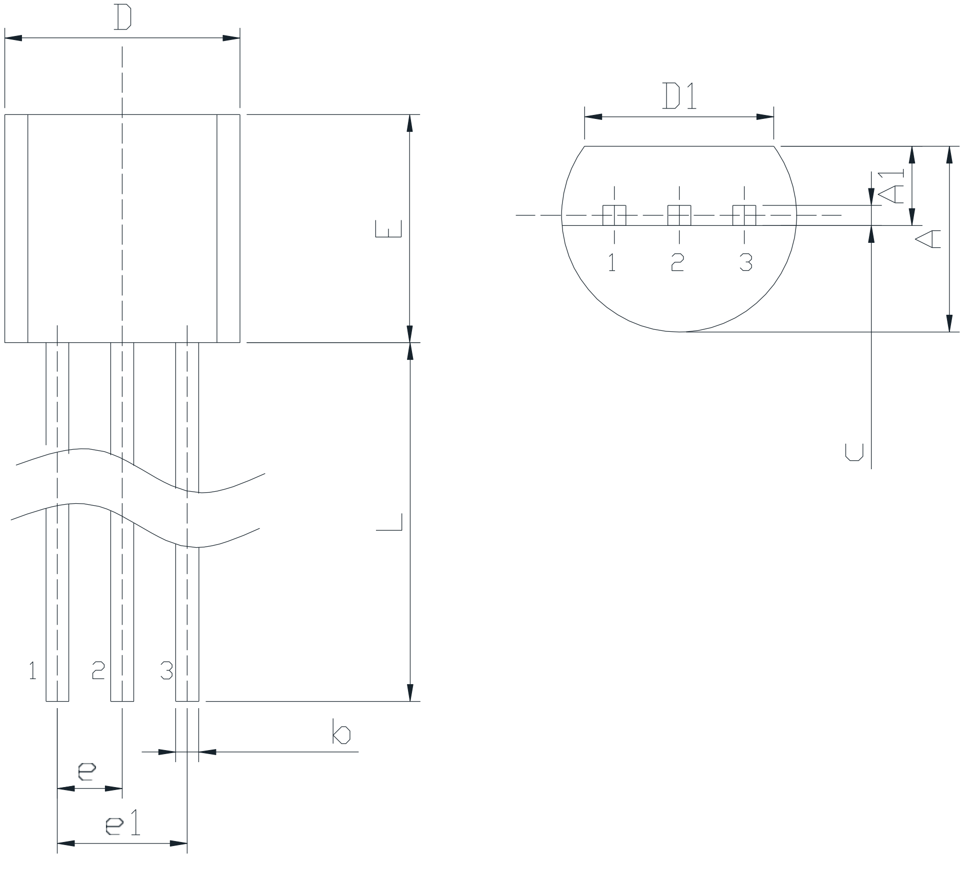
13. Package Outline Dimensions (TO-92)



Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min.	Max.	Min.	Max.
A	3.300	3.800	0.130	0.150
A1	1.100	1.400	0.043	0.055
b	0.380	0.550	0.015	0.022
c	0.300	0.510	0.012	0.020
D	4.300	4.700	0.169	0.185
D1	3.430		0.014	
E	4.300	4.700	0.169	0.185
e	1.270（TYP）		0.050（TYP）	
e1	2.540（TYP）		0.100（TYP）	
L	13.000	15.000	0.512	0.590

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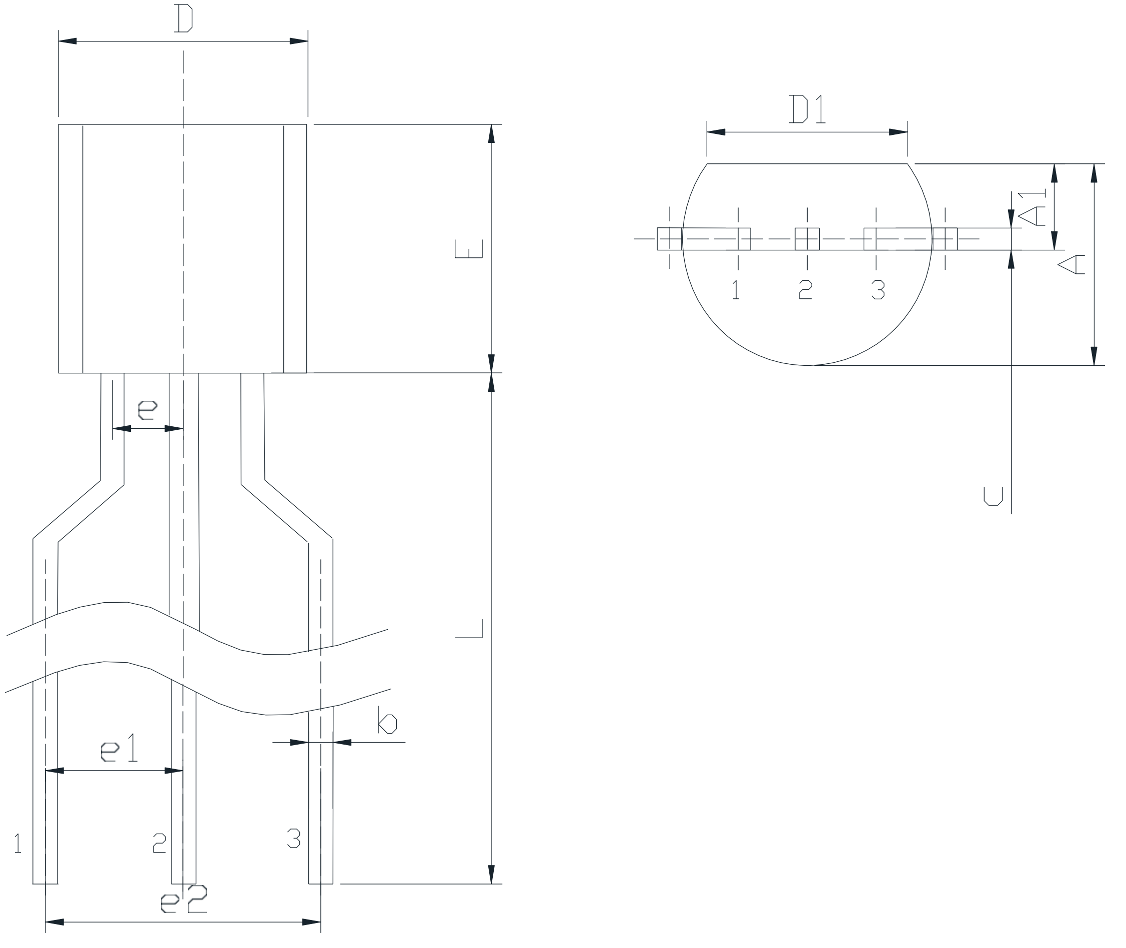
14. Package Outline Dimensions (TO-92 Bend Lead)



Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min.	Max.	Min.	Max.
A	3.300	3.800	0.130	0.150
A1	1.100	1.400	0.043	0.055
b	0.380	0.550	0.015	0.022
c	0.300	0.510	0.012	0.020
D	4.300	4.700	0.169	0.185
D1	3.430		0.014	
E	4.300	4.700	0.169	0.185
e	1.270（TYP）		0.050（TYP）	
e1	2.500（TYP）		0.098（TYP）	
e2	5.000（TYP）		0.196（TYP）	
L	13.000	15.000	0.512	0.590

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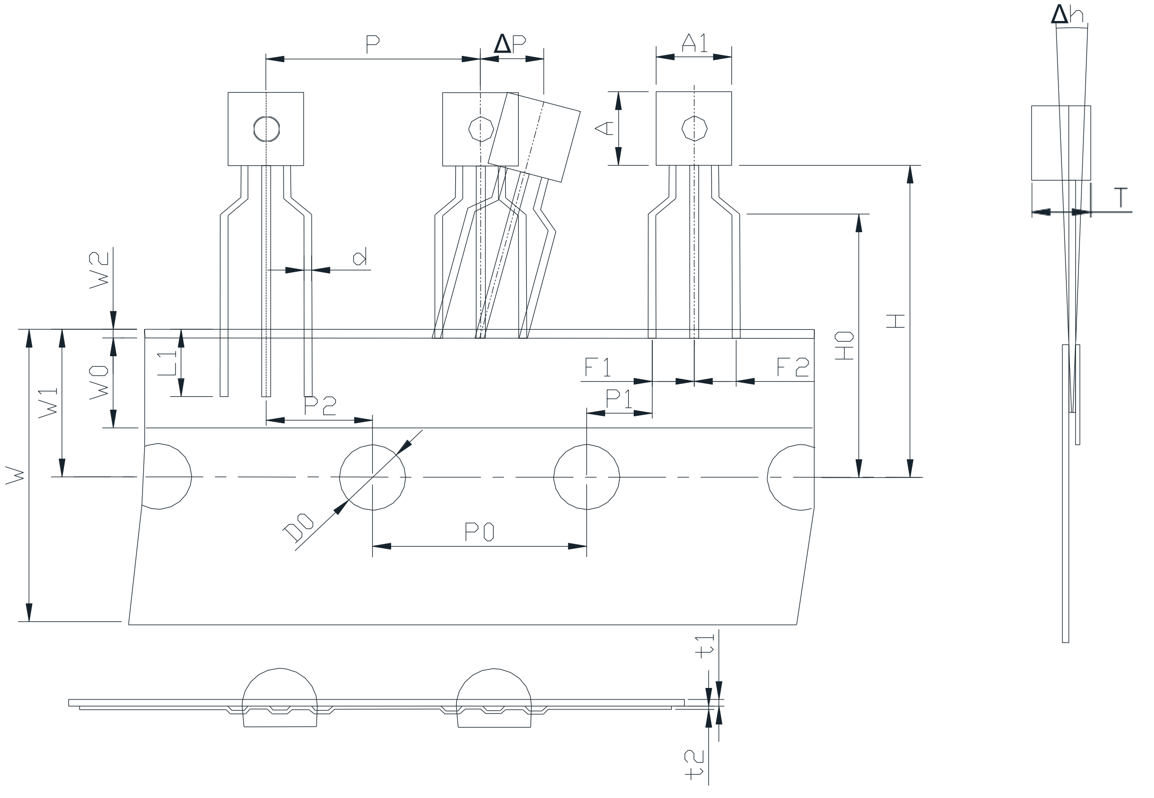
AMMO Packing Dimensions (TO-92)



Item	Symbol	Value &Tolerance
Body Width	A1	4.5±0.2
Body Height	A	4.5±0.2
Body Thickness	T	3.5±0.1
Lead Wire Diameter	d	0.46+0.09/-0.08
Pitch of Component	P	12.7±0.3
Feed Hole Pitch	P0	12.7±0.2
Hole Center to Component Center	P2	6.35±0.3
Lead to Lead Distance	F1,F2	2.5±0.3
Component Alignment, F-R	Δh	0±1.0
Type Width	W	18.0+1.0/-0.5
Hole Down Tape Width	W0	6.0±0.5

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Item	Symbol	Value &Tolerance
Hole Position	W1	9.0±0.5
Hole Down Tape Position	W2	1.0MAX
Height of Component From Tape Center	H	19.0+2.0/-1.0
Lead Wire Clinch Height	H0	16.0±0.5
Lead Wire(Tape Portion)	L1	2.5MIN
Feed Hole Diameter	D0	4.0±0.2
Taped Lead Thickness	t1	0.4±0.05
Carrier Tape Thickness	t2	0.2±0.05
Position of Hole	P1	3.85±0.3
Component Alignment	ΔP	0±1.0

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