SENSSET
SENSOR SEQUENCE

SSG-M104

MEMS Gyroscope

1. Technical parameters

Table 1.1 Technical parameter

Parameter	M104F6	M104F7	M104B1	M104B2	M104B3	M104F8	Unit
Measurement Range[1]	400	400	500	500	500	400	deg/s
Resolution	24bit						bits
Data Rate[2]	12K	12K	12K	12K	12K	12K	Hz
Group delay[3]	<3	<1.5	<1.5	<1.5	<1.5	<1	ms
@3DB	<90deg	<90deg	<90deg	<90deg	<90deg	<90deg	deg
Bandwidth (-3dB)[4]	≥90	≥180	≥200	≥200	≥200	300	Hz
Scale Factor at 25°C[5]	20000	20000	16000	16000	16000	20000	lsb/deg/s
Scale Factor Repeatability (1σ)[6]	<20	<20	<20	<20	<20	<100	ppm
Scale Factor VS Temperature (1σ)[7]	100	100	<100	<100	<100	<300	ppm
Scale Factor Non-Linearity (1σ)[8]	100	100	<150	<150	<150	<300	ppm
Bias Instability[9]	0,05	0,05	<0.1	<0.2	<0.5	<0.1	deg/hr
Bias stability @10s[10]	<0.5	<0.5	<1	<2	<5	<1	deg/hr
Bias stability @1s[11]	<1.5	<1.5	<3	<6	<15	<3	deg/hr
Angular Random Walk[12]	<0.025	<0.025	<0.05	<0.1	<0.25	<0.05	°/ √h
Bias error over temperature(1σ)[13]	<5	<5	<10	<20	<30	10	deg/Hr
Bias temperature variations, calibrated(1σ)[14]	<0.5	<0.5	<1	<5	<10	<1	deg/Hr
Bias Run-Run (1σ)[15]	<0.5	<0.5	<0.5	<2	<3	<0.3	deg/hr
Noise Peak to Peak[16]	<0.15	<0.3	<0.35	<0.4	<0.4	<0.25	deg/s
g Sensitivity[17]	<1	<1	<1	<1	<3	<1	°/hr/g
VRE[18]	<1	<1	<1	<1	<3	<1	°/hr/g (rms)
Startup Time	750ms						
Sensor Resonant Frequency	10.5k-13.5K Hz						
Shock (operating)	500g, 1ms						
Shock (survival)	10000g, 10ms						
Vibration Operating	18grms						
Operating Temperature	-40 ~ +85◦C						
Max storage (survival) Temperature	-55 ~ +125◦C						
Supply voltage	5±0.25V						
Current consumption	45mA						

1) Clockwise rotation is positive output,Clamped at ±105%FS during over-rang
2) Refresh rate of the output data at room temperature
3) Time delay between the physical input and the output signal
4) Defined as the frequency for which attenuation is >-3dB
5) factory setting
6) day by day at setting Temp(1σ)
7) Over temperature range（1σ）
8) Percentage of dynamic range using a best straight line fit
9) Allan Variance @25°C
10) 10s Allan Variance
11) 1s Allab Variance
12) Allan Variance @25°C
13) Over temperature range（1σ）
14) Over temperature range（1σ）
15) day by day at setting Temp(1σ)
16) Over the Bandwidth frequency range, at room temperature
17) Any axis, Tested over ±1g
18) 12gRMS, 20-2000 Hz

Table 1.2 Technical parameter

Parameter	M104C1	M104C2	M104D1	M104D2	M104E1	M104E2	M104A1	Unit
Measurement Range[1]	1000	1000	2000	2000	4000	4000	8000	deg/s
Resolution	24bit							bits
Data Rate[2]	12K	12K	12K	12K	12K	12K	12K	Hz
Group delay[3]	<2	<1.5	<1.5	<1.5	<1.5	<1.5	<1.5	ms
@3DB	<90deg	<90deg	<90deg	<90deg	<90deg	<90deg	<90deg	deg
Bandwidth (-3dB)[4]	≥120	≥200	≥180	≥200	≥180	200	≥180	Hz
Scale Factor at 25°C[5]	8000	8000	4000	4000	2000	2000	1000	lsb/deg/s
Scale Factor Repeatability (1σ)[6]	<20	<20	<20	<10	<10	<10	<20	ppm
Scale Factor VS Temperature (1σ)[7]	100	<100	<100	<100	<100	<100	<100	ppm
Scale Factor Non-Linearity (1σ)[8]	<100	<150	<100	<150	<100	<150	<150	ppm
Bias Instability[9]	<0.1	<0.5	<0.3	<1	<0.3	<2	<1	deg/hr
Bias stability @10s[10]	<1	<5	<2.5	<6	<5	<10	<10	deg/hr
Bias stability @1s[11]	<3	<15	<7.5	<18	<15	<30	<25	deg/hr
Angular Random Walk[12]	<0.05	<0.25	<0.15	<0.3	<0.25	<0.5	<0.5	°/ √h
Bias error over temperature(1σ)[13]	5	<30	5	<50	10	<100	10	deg/Hr
Bias temperature variations, calibrated(1σ)[14]	<1	<15	<1	<20	<2	<30	<5	deg/Hr
Bias Run-Run (1σ)[15]	<0.3	<4	<1	<5	<3	<5	<10	deg/hr
Noise Peak to Peak[16]	<0.3	<0.4	<0.5	<0.5	<1	<1	<2	deg/s
g Sensitivity[17]	<1	<3	<1	<3	<1	<3	<1	°/hr/g
VRE[18]	<1	<3	<1	<3	<1	<1	<1	°/hr/g (rms)
Startup Time	750 ms							
Sensor Resonant Frequency	10.5k-13.5K Hz							
Shock (operating)	500g, 1ms							
Shock (survival)	10000g, 10ms							
Vibration Operating	18grms							
Operating Temperature	-40 ~ +85◦C							
Max storage (survival) Temperature	-55 ~ +125◦C							
Supply voltage	5±0.25V							
Current consumption	45mA							

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Table 1.3 Technical parameter

Parameter	M104A2	M104G1	M104H1	M104H2	Unit
Measurement Range[1]	8000	10800	100	100	deg/s
Resolution	24 bit				bits
Data Rate[2]	12K	12K	2K	2K	Hz
Group delay[3]	<1.5	<1.5	<50	<6	ms
@3DB	<90deg	<90deg		<90deg	deg
Bandwidth (-3dB)[4]	200	200	12	≥50	Hz
Scale Factor at 25°C[5]	1000	720	80000	80000	lsb/deg/s
Scale Factor Repeatability (1σ)[6]	<10	<10	<100	<100	ppm
Scale Factor VS Temperature (1σ)[7]	<100	<100	<300	<300	ppm
Scale Factor Non-Linearity (1σ)[8]	<150	<100	<300	<300	ppm
Bias Instability[9]	<3	<5	<0.02	<0.02	deg/hr
Bias stability @10s[10]	<15	<20	<0.1	<0.1	deg/hr
Bias stability @1s[11]	<50	<60	<0.3	<0.3	deg/hr
Angular Random Walk[12]	<0.8	<1	<0.005	<0.005	°/ √h
Bias error over temperature(1σ)[13]	<100	100	3	5	deg/Hr
Bias temperature variations, calibrated(1σ)[14]	<30	30	<0.3	<0.5	deg/Hr
Bias Run-Run (1σ)[15]	<5	5	<0.1	<0.1	deg/hr
Noise Peak to Peak[16]	<1.5	<1.5	<0.005	<0.015	deg/s
g Sensitivity[17]	<4	<4	<1	<1	°/hr/g
VRE[18]	<1	<1	<1	<1	°/hr/g (rms)
Startup Time	750ms				
Sensor Resonant Frequency	10.5k-13.5K Hz				
Shock (operating)	500g, 1ms				
Shock (survival)	10000g, 10ms				
Vibration Operating	18grms				
Operating Temperature	-40 ~ +85◦C				
Max storage (survival) Temperature	-55 ~ +125◦C				
Supply voltage	5±0.25V				
Current consumption	45mA				

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11) 1s Allab Variance
12) Allan Variance @25°C
13) Over temperature range（1σ）
14) Over temperature range（1σ）
15) day by day at setting Temp(1σ)
16) Over the Bandwidth frequency range, at room temperature
17) Any axis, Tested over ±1g
18) 12gRMS, 20-2000 Hz

Table 2 – Electrical and mechanical parameters

Parameter	Value
Impact (charged)	1000g. 1ms
Impact resistance (uncharged)	10000g, 10ms
Vibration (charged)	18 grms, Filter spectrum
Operating temperature	-40°C~+85°C
Max storage temperature	-55°C~+125°C
Supply Voltage	5 ± 0.25 V
Current consumption	40 mA

2. Pin definition

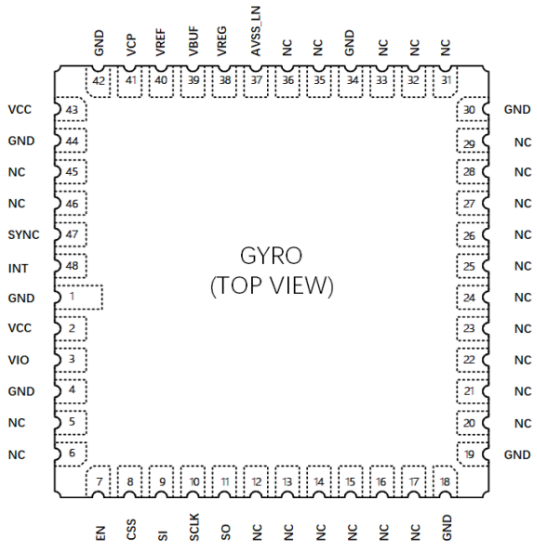

Figure 1. Pin definition

Table 3. Pin definition

Pin	Definition	Electrical properties	Supply	Note
1	GND	Ground	0V	
2	VCC	Supply	5V	Power supply voltage input, need 10uF, 0.1uF bypass capacitor arrived.
3	VIO	I/O supply	1.6V~5V	The input voltage will be used as the reference voltage of the interface, which needs to be connected with the controller The interface voltage is the same. A 0.1uF bypass capacitor is required to ground
4	GND	Ground	0V	
7	EN	Input	VIO	Chip enable. Input high to enable the chip.
8	CSS	Input	VIO	SPI chip select
9	SI	Input	VIO	SPI data input
10	SCLK	Input	VIO	SPI data input
18	SO	Output	VIO	SPI data output
19	GND	Ground	0V	
30	GND	Ground	0V	

Table 3. Pin definition (continuation)

Pin	Definition	Electrical properties	Supply	Note
34	GND	Ground	0 V	
37	AVSS_LN	Simulated	0 V	Connect to power ground via a ferrite bead
38	VREG	Reference voltage	4V~6V	Internal voltage reference, connect 1uF bypass capacitor to analog ground
39	VBUF	Reference voltage	1.65 V	Internal voltage reference, connect 1uF bypass capacitor to analog ground
40	VREF	Reference voltage	2.4 V	Internal voltage reference, connect 0.1uF and 0.01uF bypass capacitors to Simulated
41	VCP	Reference voltage	11 V	Internal voltage reference, connected to 1uF (withstand voltage greater than 16V) bypass circuit to the ground
42	GND	Ground	0 V	
43	VCC	Power Supply	5 V	Power supply voltage input, need 10uF, 0.1uF bypass capacitor arrived.
44	GND	Ground	0 V	
47	SYNC	Input	VIO	Sampling synchronization signal input, can be left floating when not in use.
48	INT	Output	VIO	Interrupt signal output, can be suspended when not in use.

3. Wiring diagram

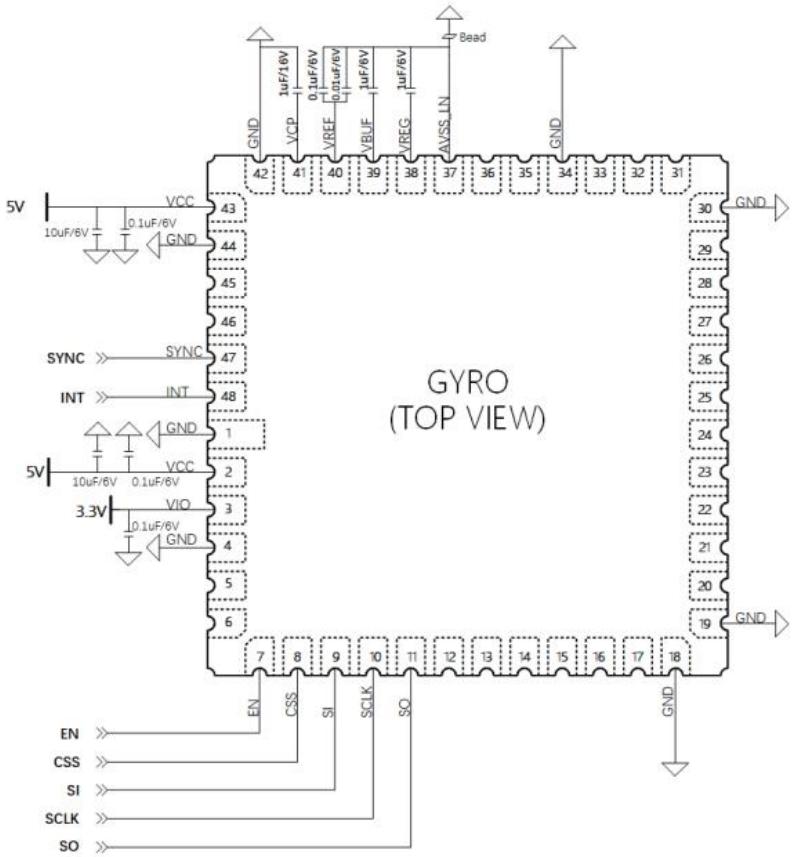

Figure 2. Wiring Diagram

- The decoupling capacitors of pins VCP, VREF, VBUF, and VREG should be placed as close as possible to the pins and minimized The equivalent resistance of the trace.
- The other end of the decoupling capacitor of VREF, VBUF and VREG is connected to AVSS_LN nearby, and then connected to signal ground.
- The decoupling capacitors of VCC and VIO should also be placed close to the corresponding pins. When VCC is working normally, the overall current will be there is about 35mA, and a wide PCB trace is required to ensure a stable voltage.
- To make the device assembly flat, try to avoid traces under the package.
- When arranging the position of the device, try to avoid the stress concentration area. It is necessary to avoid large heat dissipation elements, areas that are squeezed and pulled by external mechanical contact, and areas that are prone to warping during overall installation, such as set screws.

4. Communication and control

4.1 Hardware interface

4.1.1 SPI timing

SSG-M104 sensor data is achieved by accessing and reading the specified register address. Likewise, the control of the SSG-M104 Implemented by writing a value to the specified register.

SSG-M104 implements register access through the 4-wire SPI hardware interface sequence, and writes or reads the register at the specified address.

The SPI interface of SSG-M104 adopts Mode 3 timing type for slave mode. That is, CPOL = 1, CPHA = 1, CS pulls

Before low, the default level of Clock is high, and the data is read on the rising edge.

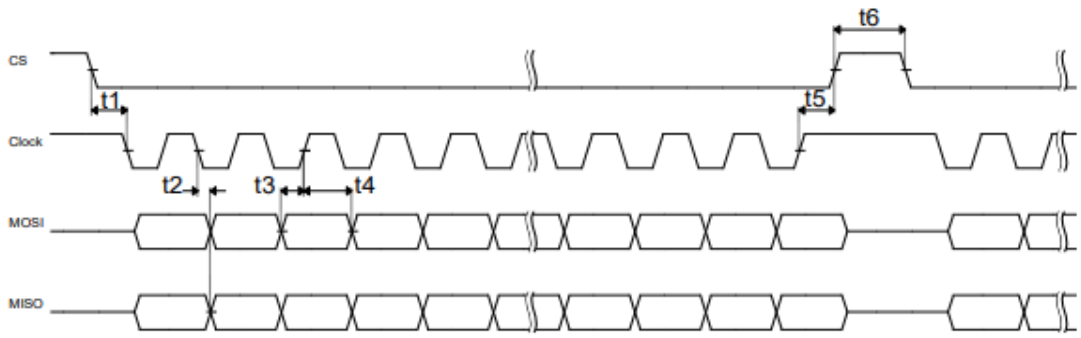

Figure 3. SPI Timing parameters

Table 4. Timing parameters

Symbol	Parameter	Condition	Min	Average	Max	Value
Fsclk	SPI clock frequency	DIN/DOUT maximum load 20pF		4	8	MHz
T1	Chip select to clock edge		200			ns
T2	DOUT valid time after CLK edge					ns
T3	Before the rising edge of SCLK DIN build time for		10			ns
T4	DIN hold time after SCLK rising edge		10			ns
Tdr, Tdf	DOUT rise and fall times, shown in the graph	VIO 3.3 V		10		sn
t5	SSB high time after SCLK edge		200			ns
T6	Interval between two SPI accesses		500			ns

4.1.2 Read and write control

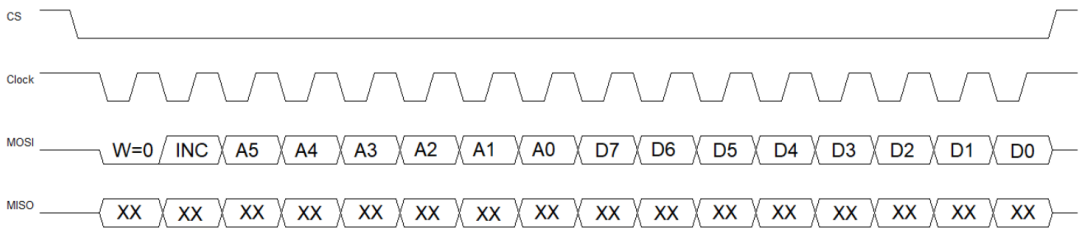

Figure 4. SPI single-byte write timing

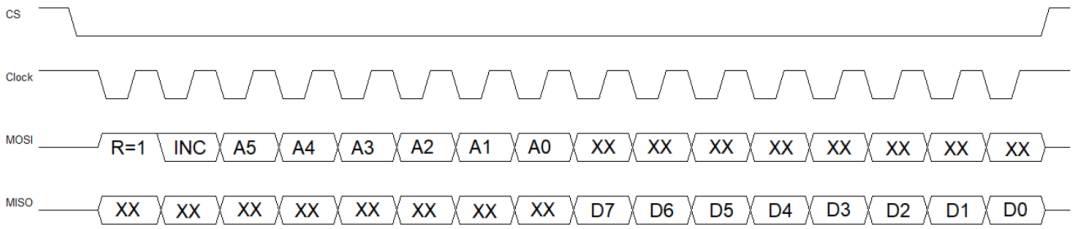

Figure 5. SPI Single-byte read timing

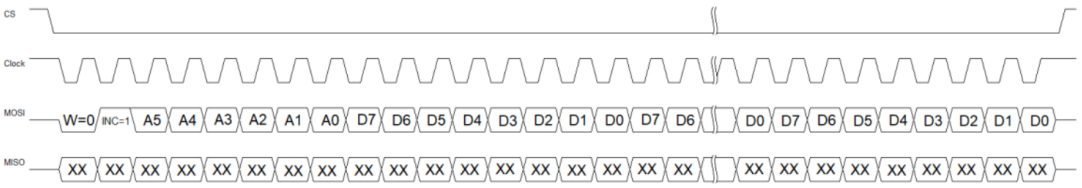

Figure 6. SPI Multibyte write timing

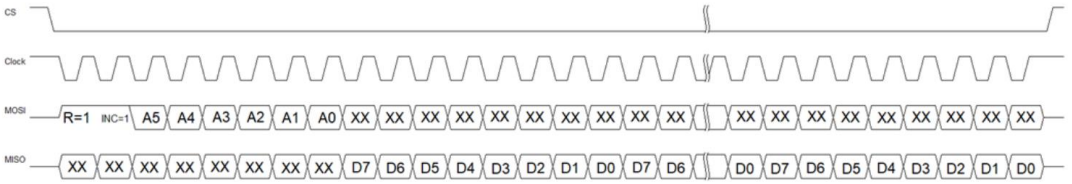

Figure 7. SPI Multibyte read timing

4.2 Register description

4.2.1 Introduction to register format

SSG-M104 register address (absolute address) is composed of "page" and "address offset" when accessing. "page" is a single byte, available the value range is 0~1. The address offset is 6 bits, and the range is 0x00~0x3E. 0x3F is used as the "page" setting register address. This address is only mapped to page 0 and is not affected by the "page" setting.

When the absolute address of the register exceeds 0x3F, the register page needs to be modified. Write the corresponding "page" value to the register page's

Set in address 0x3F.

Table 5. Register format, page 0

00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	Offset address
00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	Register address
10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F	Offset address
10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F	Register address
20	21	22	23	24	25	26	27	28	29	2A	2B	2C	2D	2E	2F	Offset address
20	21	22	23	24	25	26	27	28	29	2A	2B	2C	2D	2E	2F	Register address
30	31	32	33	34	36	36	37	38	39	3A	3B	3C	3D	3E	3F	Offset address
30	31	32	33	34	35	36	37	38	39	3A	3B	3C	3D	3E	3F	Register address

Table 6. Register format, page 1

00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	Offset address
40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	Register address
10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F	Offset address
50	51	52	53	54	55	56	57	58	59	5A	5B	5C	5D	5E	5F	Register address
20	21	22	23	24	25	26	27	28	29	2A	2B	2C	2D	2E	2F	Offset address
60	61	62	63	64	65	66	67	68	69	6A	6B	6C	6D	6E	6F	Register address
30	31	32	33	34	35	36	37	38	39	3A	3B	3C	3D	3E	3F	Offset address
70	71	72	73	74	75	76	77	78	79	7A	7B	7C	7D	7E	7F	Register address

The default register page is page 0, which can access the contents of the absolute address range of the register 0x00~0x3F.When neededFor registers whose absolute address exceeds 0x3F, the page register (0x3F) needs to be modified first, and then accessed according to the offset address.For example: if you need to access the absolute register address 0x40, you need to write the address 0x3F to 0x01 through SPI, and thenSPI operation address 0x00.Note: Since some bits in the register are defined as reserved, there are usually default values on their bits, and it is possible.

4.2.2 Introduction to register format

Register absolute address: 0x2E, STATUS

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	Data_Rdy	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

Register absolute address: 0x30, TIMP_OUT_L

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Temp_OUT [7:0]							

Register absolute address: 0x31, Rate_OUT_L

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Rate_OUT [7:0]							

Register absolute address: 0x32, Rate_OUT_M

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Rate_OUT [15:8]							

Register absolute address: 0x33, Rate_OUT_H

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Rate_OUT [23:16]							

Register absolute address: 0x3F, Addr_Page_Sel

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Addr_Page_Sel [7:0]							

Register absolute address: 0x49, Chip iD 1

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CHIP_ID_1: 0x41							

Register absolute address: 0x4A, Chip ID 2

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CHIP_ID_2: 0x01							

Register absolute address: 0x4C, OTP_ID_0

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OTP_ID_0							

Register absolute address: 0x4D, OTP_ID_1

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OTP_ID_1							

Register absolute address: 0x4E, OTP_ID_2

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OTP_ID_2							

Register absolute address: 0x4F, OTP_ID_3

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OTP_ID_3							

Register absolute address: 0x50, OTP_ID_4

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OTP_ID_4							

Register absolute address: 0x51, OTP_ID_5

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OTP_ID_5							

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Sync_ODR_Sel	BW_Sel

External sync and output bandwidth setting options.

Sync_ODR_Sel, external synchronization input parameter selection,
0: The synchronization input and update rate parameters adopt the synchronization setting register value;
1: Synchronous input and update rate parameters use OTP programming content;
BW_Sel, output bandwidth parameter selection,
0: The output bandwidth parameter adopts the bandwidth setting register value;
1: The output bandwidth parameter adopts OTP burning content;

Register absolute address: 0x6A, SYNC_CTRL

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	ODR_RATE [2:0]			DRY_Polar	Sync_Polar	Sync_Mode [1:0]	

Data update rate: ODR_RATE: 0: 2000 Hz 1: 1000 Hz 2: 500 Hz	3: 250 Hz 4: 125 Hz 5: 62.5 Hz 6: 6000 Hz 7: 12000 Hz
Synchronization input control. DRY_Polar: Data Ready output interrupt polarity.	0: When the data is valid, the interrupt pin output is low; 1: When the data is valid, the interrupt pin output is high;
Sync_Polar: External sync input signal polarity.	0: Falling edge is valid; 1: Rising edge is valid;
Sync_Mode: Synchronization signal source selection	0: Using internal synchronization signal; 1: Using an external synchronization signal;

Register absolute address: 0x6B, SYNC_DIV_L

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SYNC_DIV [7:0]							

Register absolute address: 0x6C, SYNC_DIV_H

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SYNC_DIV [15:8]							

Synchronous signal input frequency division factor High byte.
External synchronization signal frequency division factor, input range: 0~65535;
With external sync signal, ODR frequency:

$$ODR = \frac{External\ Synchronization\ Clock\ Frequency}{(DIV + 1) \cdot 2}$$

That is: when the frequency division factor is 0, the ODR is half of the frequency of the external synchronous clock.

Register absolute address：0x6D_RW_CTRL

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	Reserved	LPF SEL[1:0]		BW_CRTL[3:0]			
Low-pass filter stage selection: LPF_ODR: 0: Enable LPF 1 1: Enable LPF 1 and LPF 2 2: Enable LPF 1, LPF 2 and LPF 3 3: Disable all low pass filters							
Output bandwidth control. BW_CTRL: 0: 12.5 Hz 1: 25 Hz 2: 50 Hz 3: 100 Hz 4: 150 Hz 5: 200 Hz 6: 250 Hz 7: 300 Hz				8: 350 Hz 9: 400 Hz 10: 450 Hz 11: 500 Hz 12: 550 Hz 13: 600 Hz 14: 700 Hz 15: 800 Hz			

5. Output bandwidth

5.1 Sensor Data Format

The temperature data is 16bit wide, in two's complement format, and the highest bit is the sign bit. Register 0x30 (TEMP_OUT_L) It is the low byte of the temperature sensor output, register 0x31 (TEMP_OUT_H) is the high byte of the temperature sensor output.

The corresponding relationship between the temperature sensor value and the actual temperature can be roughly as follows formula:

$$Actual\ temperature(°C) = \frac{Temperature\ code(DEC) + 8000}{320} + 22$$

It should be noted that the output signal of the temperature sensor is usually used as a compensation parameter, so only relative accuracy is required, and the temperature sensor is inside the chip, and the actual temperature is mainly affected by the self-heating of the temperature. Therefore, the output of the temperature sensor is not corrected for the accurate Celsius temperature value. According to public the actual Celsius temperature obtained by the formula can only be used as a rough reference, and the ambient temperature of the environment where the chip is located cannot be measured.

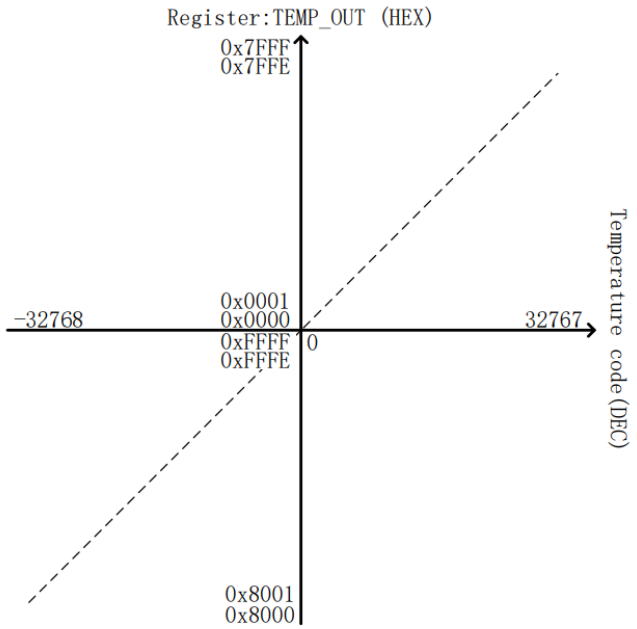

Figure 8.

5.2 Angular velocity data output

Angular velocity data is 24bit wide, two's complement format, the most significant bit is the sign bit. Register 0x32 (Rate_OUT_L)

It is the low byte of angular velocity output, register 0x33 (Rate_OUT_M) is the middle byte of angular velocity output, register 0x34 (Rate_OUT_H) is the high byte of angular velocity output.

The corresponding relationship between the value of the angular velocity sensor and the actual angular velocity can be as follows: According to the following formula:

$$angular\ velocity(^\circ / s) = \frac{Rate\ out\ code(DEC)}{scale\ \ factor}$$

Because of the product customization process. In the formula, the scale factor needs to refer to the quality inspection report when the product is shipped.

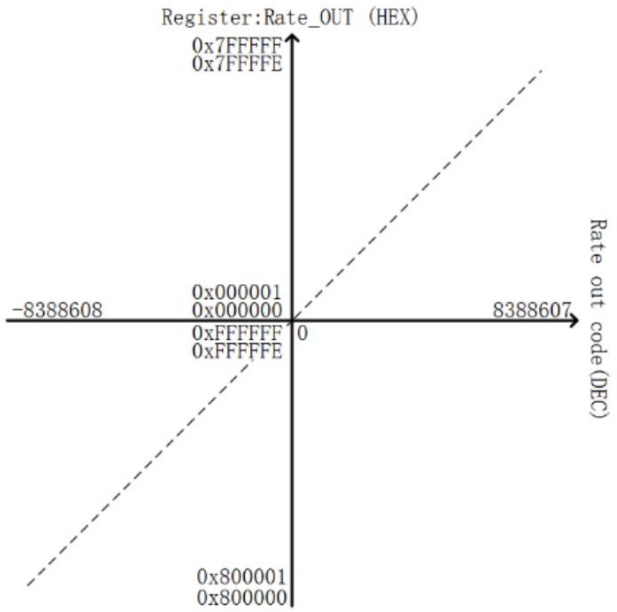

Figure 9.

5.3 Data read

The output data of SSG-M104 is stored in 5 register addresses (2-byte temperature data, 3-byte angular velocity data). When data is updated, these 5 registers are updated according to the corresponding byte order. In this process, in order to ensure that the read the register is the new data of the same frame, to avoid reading incomplete data, it is necessary to judge the valid flag of the data (STATUS, 0x2E [6]: Data_Rdy). When the data in the register is valid, the bit will be set to 1 and keep until the temperature of 0x30 ~ 0x34. After all the data in the and angular velocity data registers are read, the flag will be automatically cleared.

The recommended process for reading data is to judge the STATUS first, 0x2E[6]: The status of Data_Rdy.When it is determined that the data is valid, thenRead the sensor data 0x30~0x34.It should be noted that, To read the status register STATUS, 0x2E[6]:Data_Rdy is requiredTo be completed in a separate SPI reading process, it cannot be combined with the data inIt is completed in a continuous SPI read operation.

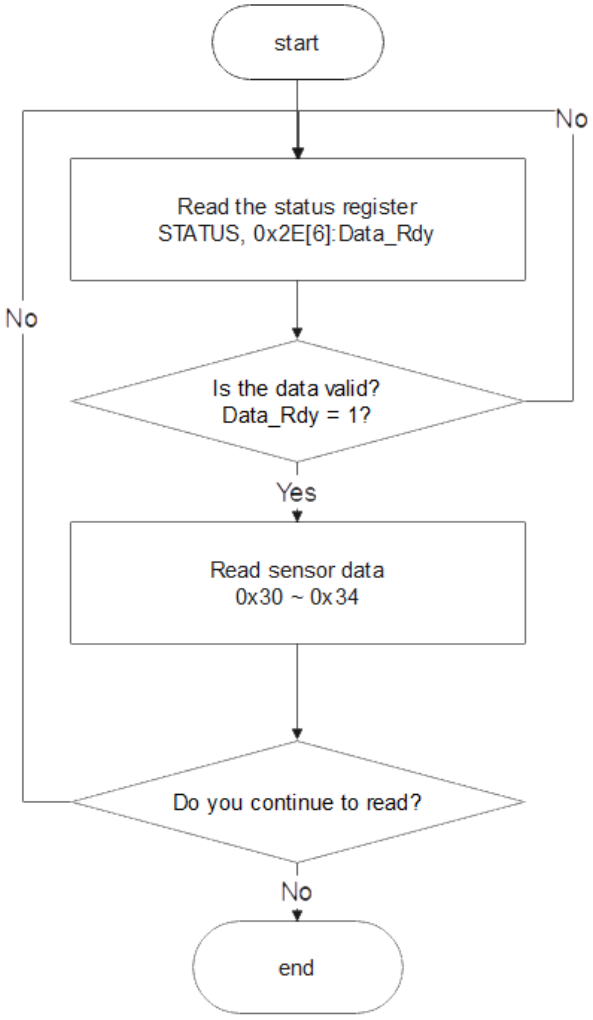

Figure 10.

6 Output control

6.1 Operation instructions for switching the curing configuration to register control

Part of the control of SSG-M104 is open to customers, and customized adjustment operations can be carried out.If you need to modify this part ofSetting, the relevant module control needs to be switched from the cured configuration to the register control state.

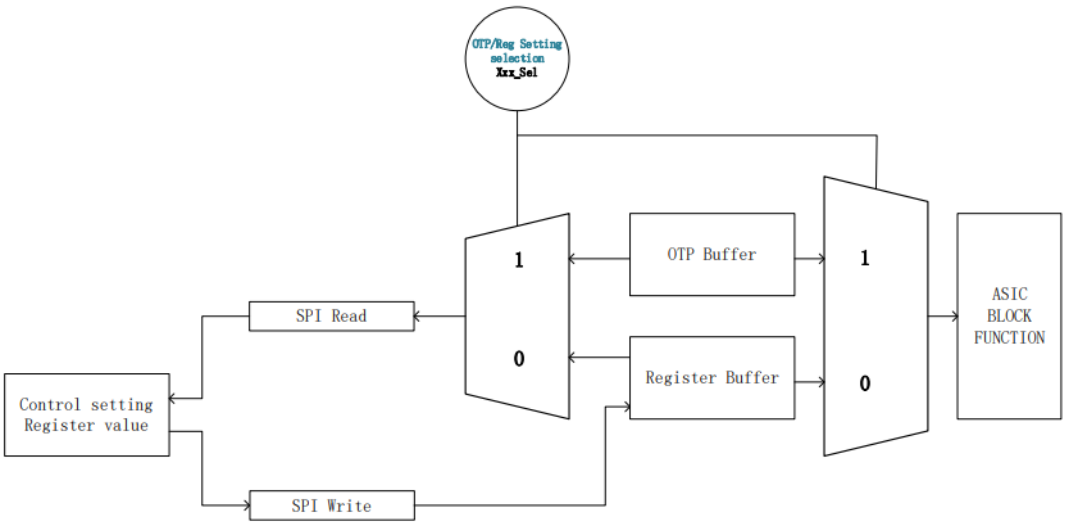

Figure 11.

The writing of control parameters should be applied to the device module, and the selection control bits of the corresponding module need to be configured.The read-back of the control parameters of the corresponding module will also be distinguished according to the corresponding selection of control bits.Therefore, the parameters of the device function module should beWhen making changes, you need to read the current register value back through the SPI, modify the corresponding control, write, and then modify the mode.The selection control bit of the block parameter.

6.2 Output signal filter setting

The bandwidth of the SSG-M104 output signal can be adjusted according to demand.The adjustment range is 12.5Hz ~800Hz.A small output bandwidth helps to improve the noise of the output signal, but at the same time reduces the response of the high-frequency signal and increases the delay of the signal output.The specific settings need to be adjusted according to specific needs.The parameters of SSG-M104 are generally factory cured.Therefore, if you need to adjust the output signal bandwidth and filter stageNumber, then follow the steps below.

6.2.1 Output bandwidth setting

1) Read the value of BW_CTRL (0x6D) and record it.
2) BW_CTRL(0x6D)[3:0]: BW_CRTL[3:0], set the parameters to modify the corresponding bit.Pay attention to keep the rest of the bitsThe bit value remains unchanged.Write the new value to register BW_CTRL (0x6D)
3) Read the value of SYNC_BW_SEL (0x59) and record it.
4) SYNC_BW_SEL (0x59) [0]: BW_Sel, set to 0.Set the parameters to modify the corresponding bit.Pay attention to retentionThe value of the remaining bits remains unchanged.Write the new value to SYNC_BW_SEL (0x59)

6.2.2 Modify the output filter stage

1) Read the value of BW_CTRL (0x6D) and record it.
2) BW_CTRL(0x6D)[5:4]: LPF_SEL[1:0], set the parameter to modify the corresponding bit.Pay attention to keep the rest of the bitsThe bit value remains unchanged. Write the new value to register BW_CTRL (0x6D)
3) Read the value of SYNC_BW_SEL (0x59) and record it.
4) SYNC_BW_SEL (0x59) [0]: BW_Sel, set to 0.Set the parameters to modify the corresponding bit.Pay attention to retention the value of the remaining bits remains unchanged.Write the new value to SYNC_BW_SEL (0x59)

6.3 Data update rate

In the case of using internal synchronization to update data, the data update rate can be adjusted by modifying the data update rate register.If you need to change the data update rate, follow the steps below.

1) And output signals SYNC_BW_SEL (0x59), SYNC_CTRL (0x6A) and output.
2) SYNC_CTRL (0x6A) [6:4]: ODR_RATE, select the required data update rate.Set and modify the corresponding bitThe parameters.Note that the remaining bit values are left unchanged.
3) SYNC_BW_SEL (0x59) [1]: Sync_ODR_Sel, set to 0, the synchronization signal selection has a register configuration decisionset.Set the parameters to modify the corresponding bit.Note that the remaining bit values are left unchanged.
4) Write a new value to the register SYNC_BW_SEL (0x59)

6.4 Output synchronization

SSG-M104 supports the use of external synchronization signals to synchronize the output.The requirement for the synchronization signal is a square wave with a 50% duty cycle.The input frequency is at least twice the required ODR.By default, the internal synchronous clock is used to control the ODR.If you need to use an external synchronization input, pressFollow the steps below.

1. Read out register SYNC_BW_SEL (0x59), SYNC_CTRL (0x6A), SYNC_DIV_H(0x6C), SYNC_DIV_L(0x6B) and write.
2. SYNC_DIV_H(0x6C), SYNC_DIV_L(0x6B):SYNC_DIV, Set the frequency division system of the input synchronization signalnumber. Write a new value to the register SYNC_DIV_H (0x6C) and SYNC_DIV_L(0x6B);
3. SYNC_CTRL(0x6A)[2]: Sync_Polar, the choice is to use the rising edge or the falling edge as the synchronization edge.Set upModify the parameters of the corresponding bit. Note that the remaining bit values are left unchanged.
4. SYNC_CTRL(0x6A)[1:0]: Sync_Mode [1:0], set to 1, choose to use an external synchronization signal input. Set the parameters to modify the corresponding bit. Note that the remaining bit values are left unchanged.
5. Write a new value to the register SYNC_CTRL(0x6A);
6. SYNC_BW_SEL (0x59) [1]: Sync_ODR_Sel, set to 0, Synchronization signal selection has register configuration decisionset.Set the parameters to modify the corresponding bit. Note that the remaining bit values are left unchanged.
7. Write a new value to the register SYNC_BW_SEL (0x59)

In the setting, the number of dividers of the input signal is 0, then the input signal is divided by 2 and generated as an output control signal. ODR.The specific calculation formula is as follows:

$$ODR = \frac{External\ synchronous\ clock\ frequency}{(DIV + 1) \cdot 2}$$

Before modifying the relevant control bits of the register, the corresponding parameter register needs to be read out first, and then written after modifying the corresponding bits., Then modify the relevant control bits of the register and switch to the register control state.

7. Reference suggestion

7.1 Welding recommendations

Please refer to IPC/JEDEC J-STD-020D.1. The curve of reflow soldering depends not only on the sensor, but also on the PCBplate.In order to improve welding reliability, it is recommended to use the coefficient of thermal expansion (CTE) and the gyroscope package (6.8ppm /°C) expansionPlates with close coefficients.The following materials are excerpted from IPC/JEDEC J-STD-020D.1

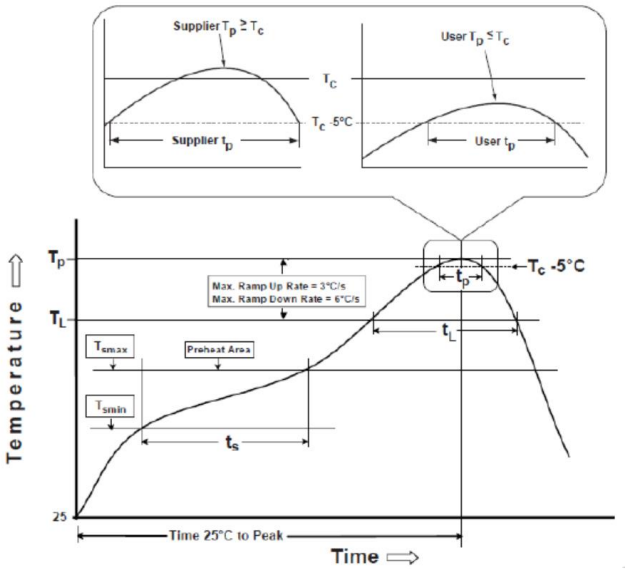

Figure 12. Reflow curve (JEDEC)

Table 7. Recommended reflow temperature curve (JEDEC)

Parameter	Sn – Pb welding	Lead-free welding
Average rise rate t_{SMAX} to t_P	Maximum 3ºC/seconds	Maximum 3°C/sec
Warm up	100ºC	100ºC
Minimum temperature value (Tsmin)	150ºC	200ºC
Maximum temperature value (Tsmax)		
Time (ts)	60-120 s	60-180 s
Time maintenance	183ºC	217ºC
Temperature (Tl)	60-150 s	60-150 s
Time (tl)		
Peak temperature (T_0)	240ºC (+/- 5ºC)	260ºC (+/-5ºC)
Actual peak temperature (tp) retention time at 5°C	10-30 s	10-40 s
Decline rate	Maximum 6°C/sec	Maximum 6°C/sec
25°C to peak temperature time	Maximum 6 minutes	Maximum 8 minutes

7. Mechanical Dimension

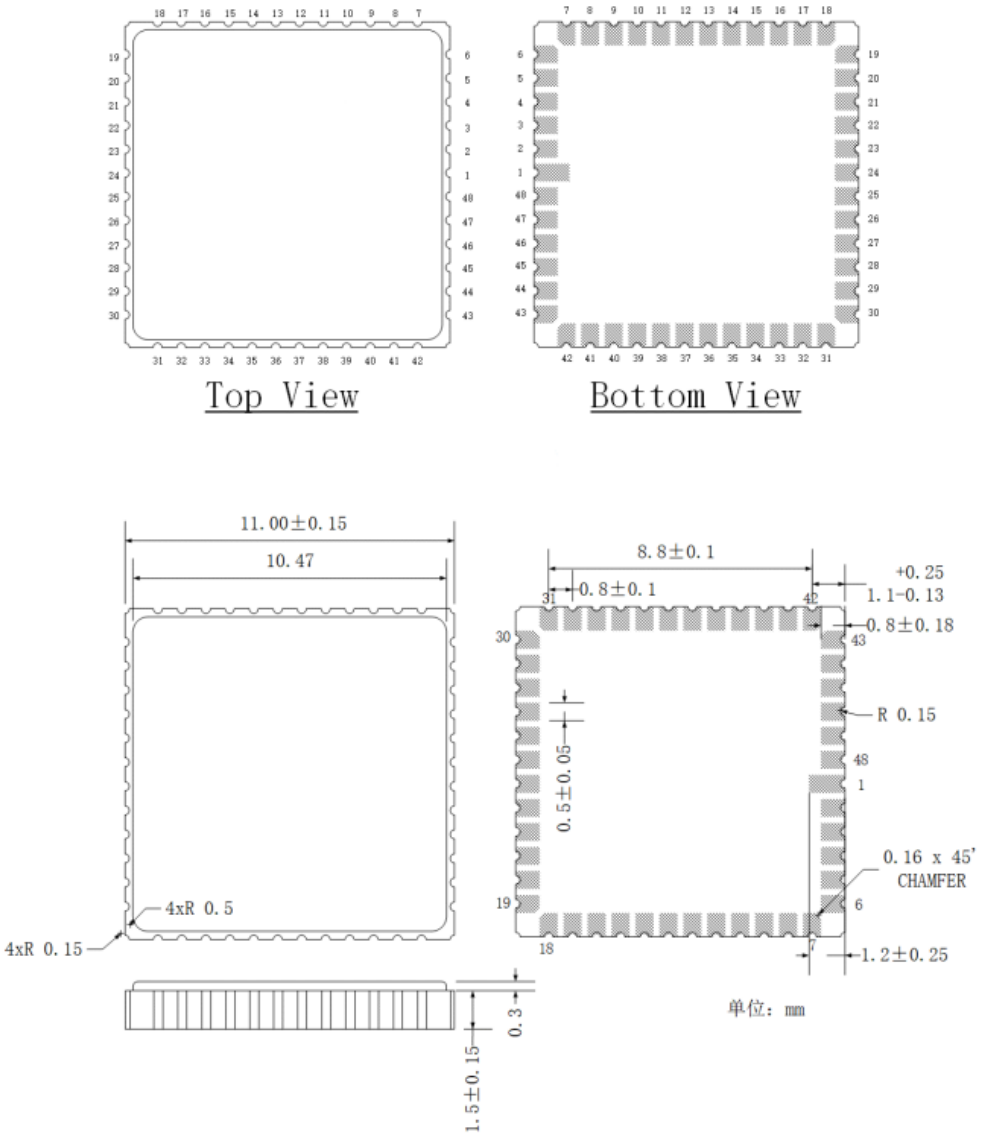

Figure 13. Mechanical Dimension

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