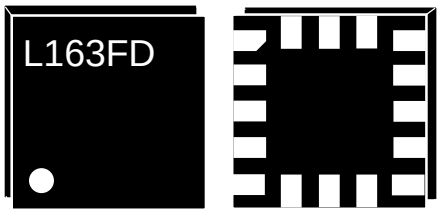
SENSSET
SENSOR SEQUENCE

SSA-L163FD

Low-power high performance 3-axes accelerometer



LGA - 16 (3x3x0.95 mm)

PRODUCTS FEATURES

- Supply voltage, 1.62V to 3.6V
- For 3*3*0.9 mm LGA-16 package
- User selectable range, ±2g, ±4g, ±8g, ±16g
- User selectable data output rate
- Digital I2C/SPI output interface
- 14 bit resolution
- Low power consumption
- 2 Programmable interrupt generators with independent function for motion detection
- Free-fall detection
- Factory programmable offset and sensitivity
- RoHS compliant

1. Internal schematic diagram and pin description

1.1. Block diagram

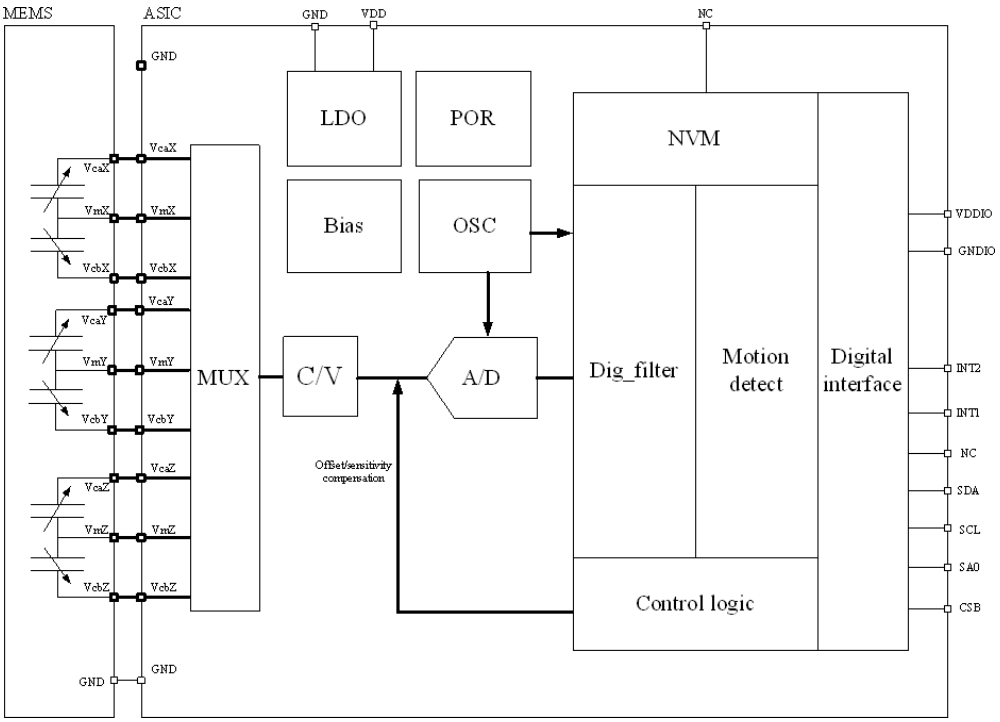


Figure 1.1. Block diagram

1.2. Pin description

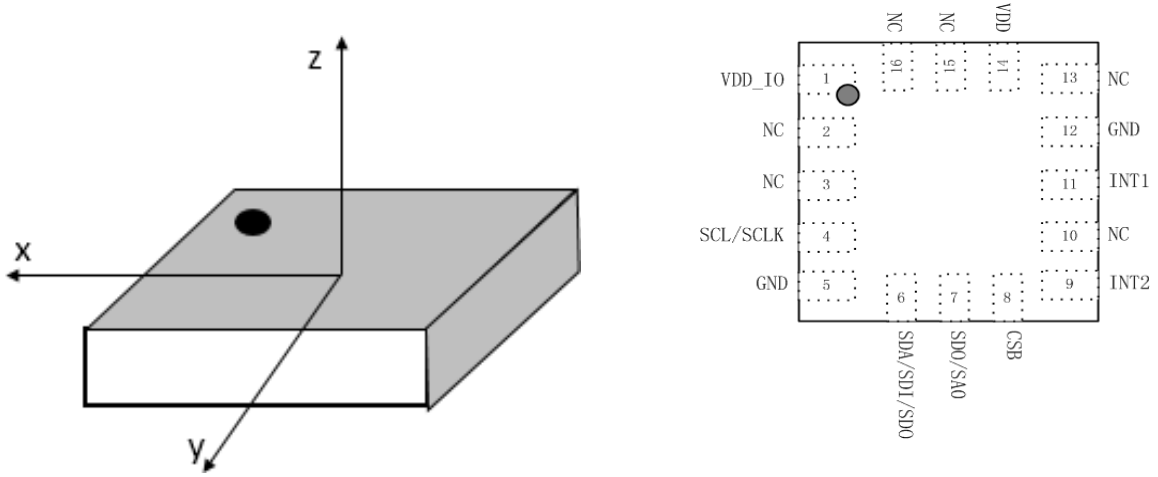


Figure 1.2. Pin description

Table 1. Pin description

Pin number	Name	I/O Type	Function
1	VDD_IO	Supply	Power supply for I/O pins
2	NC	----	Not connected
3	NC	----	Not connected, This pin must be floating or connected to GND
4	SCL SCLK	Digital in	I2C serial clock (SCL) SPI serial port clock (SCLK)
5	GND	Ground	0V supply
6	SDA SDI SDO	Digital I/O	I2C serial data (SDA) SPI serial data input (SDI) 3-wire interface serial data output (SDO)
7	SDO SA0	Digital out	SPI serial data output (SDO) I2C less significant bit of the device address (SA0)
8	CSB	Digital in	Chip select for SPI When using the I2C communication, CS pin must be connected to VDDIO or floating
9	INT2	Digital out	Inertial interrupt 2
10	NC	----	Not connected
11	INT1	Digital out	Inertial interrupt 1
12	GND	Ground	0 V supply
13	NC	----	Not connected
14	VDD	Supply	Power supply
15	NC	----	Not connected
16	NC	----	Not connected

2. Mechanical and electric characteristics

2.1. Mechanical characteristics

Table 2. Mechanical characteristics (VDD = 2.5V, T = 25°C unless otherwise noted)

Symbol	Parameter	Test conditions	Min	Type	Max	Unit
FS	Measurement range	FS bit set to 00		±2		g
		FS bit set to 01		±4		g
		FS bit set to 10		±8		g
		FS bit set to 11		±16		g
So	Sensitivity	FS bit set to 00		4096		LSB/g
		FS bit set to 01		2048		LSB/g
		FS bit set to 10		1024		LSB/g
		FS bit set to 11		512		LSB/g
TCSo	Sensitivity change vs. temperature	FS bit set to 00		±0.01		%/°C
Tyoff	Typical zero-g level offset accuracy			±70		mg
Tcoff	Zero-g level change vs. temperature	Max delta from 25°C		±0.6		mg/°C
An	Acceleration noise density	FS bit set to 00, Normal Mode, ODR = 125Hz		200		ug/sqrt(Hz)
XY noise	XY STDEVA noise	FS bit set to 00, Normal Mode, ODR = 125Hz		2.2		mg
Z noise	Z STDEVA noise	FS bit set to 00, Normal Mode, ODR = 125Hz		3.8		mg
Top	Operation temperature range		-40		85	℃

2.2. Electrical characteristics

Table 3. Electrical characteristics (Vdd = 2.5V,T = 25°C unless otherwise noted)

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
VDD	Supply voltage		1.62	2.5	3.6	V
VDD_IO	I/O Pins supply voltage		1.62		VDD	V
IDD	current consumption in normal mode	Top=25℃, ODR=1kHz		180		uA
IDD_LP	current consumption in low power mode	Top=25℃, ODR=62.5Hz BW=500Hz		40		uA
IDD_SM	current consumption in suspend mode	Top=25℃		0.7		uA
VIH	Digital high level input voltage	SPI&I2C	0.7*Vdd_IO			V
VIL	Digital low level input voltage	SPI&I2C			0.3*Vdd_IO	V
VOH	high level output voltage		0.9*Vdd_IO			V
VOL	Low level output voltage				0.1*Vdd_IO	V
BW	System bandwidth		1.95		500	Hz
ODR	Output data rate		1		1000	Hz
TWU	Wake-up time	From stand-by		1		ms
TSU	Start-up time	From power off		3		ms
PSRR	Power Supply Rejection Rate	Top=25℃			20	mg/V

2.3. Absolute maximum ratings

Table 4. Absolute maximum ratings

Parameter	Test conditions	Min	Max	Unit
Storage Temperature		-45	125	℃
Supply Voltage VDD	Supply pins	-0.3	4.25	V
Supply Voltage VDD_IO	Logic pins	-0.3	Vdd_IO+0.3	V
ESD Rating	HMB,R=1.5k,C=100pF		±2	kV
Mechanical Shock	Duration<200us		10,000	g

**Note: Supply voltage on any pin should never exceed 4.25V*

3. Communication interface Electrical specification

3.1.1. SPI Electrical specification

Table 5. Electrical specification of the SPI interface pins

Symbol	Parameter	Condition	Min	Max	Unit
fsclk	Clock frequency	Max load on SDIO or SDO = 25pF		10	MHz
t_{SCKL}	SLCK low pulse		20		
t_{SCKH}	SLCK high pulse		20		
t_{SDI_setup}	SDI setup time		20		ns
t_{SDI_hold}	SDI hold time		20		ns
t_{SDO_OD}	SDO/SDI output delay	Load = 25pF		30	ns
		Load = 250pF		40	ns
t_{CSB_setup}	CSB setup time		20		ns
t_{CSB_hold}	CSB hold time		40		ns

The figure below shows the definition of the SPI timing given in the above table:

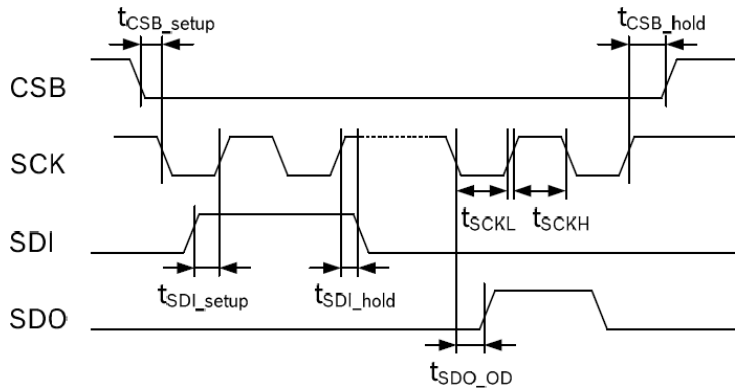


Figure 3.1.1. SPI slave timing diagram

3.1.2 I2C Electrical specification

Table 6. Electrical specification of the I2C interface pins

Symbol	Parameter	Min	Max	Unit
f_{scl}	Clock frequency		400	kHz
t_{LOW}	SCL low pulse	1.3		us
t_{HIGH}	SCL high pulse	0.6		us
t_{SUDAT}	SDA setup time	0.1		us
t_{HDDAT}	SDA hold time	0.0		us
t_{SUSTA}	Setup Time for a repeated start condition	0.6		us
t_{HDSTA}	Hold time for a start condition	0.6		us
t_{SUSTO}	Setup Time for a stop condition	0.6		us
t_{BUF}	Time before a new transmission can start	1.3		us

The figure below shows the definition of the I2C timing given in the above table:

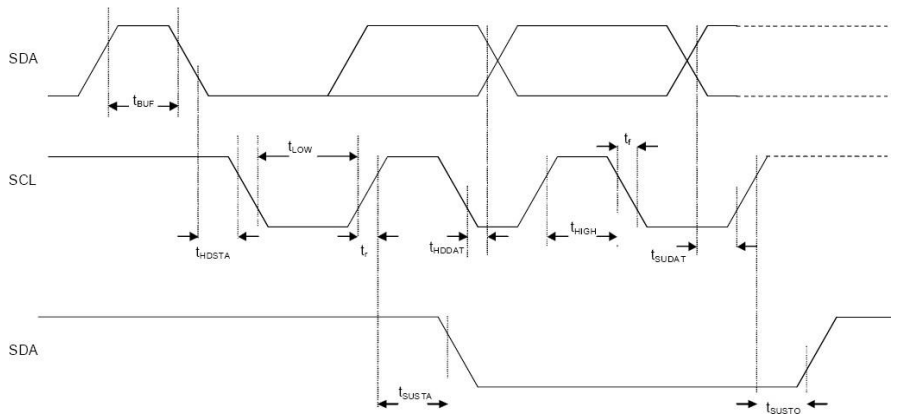


Figure 3.1.2. SPI slave timing diagram

3.2. Digital interface operation

The SSA-L163FD supports two serial digital interface protocols for communications as slave with a host device: SPI and I2C. The active interface is selected by the state of the pin CS, 0 selects SPI and 1 selects I2C. By default, SPI operates in 3-wire mode and it can be re-configured by writing 1 to bit 'SDO_active' to work in 4-wire mode. Both interfaces share the same pins. The mapping for each interface is given in the following table:

Table 7. Mapping of the interface pins

PIN name	I2C	SPI
SCL/SCLK	Serial clock	Serial clock
SDA/SDI	Serial Data	Data input (4-wire mode). Data input/output (3-wire mode)
SA0/SDO	Used to set LSB of I2C address	Data output (4-wire mode)
CSB	Unused	Chip select

3.2.1. SPI Operation

The falling edge of CSB, in conjunction with the rising edge of SCLK, determines the start of framing. Once the beginning of the frame has been determined, timing is straightforward. The first phase of the transfer is the instruction phase, which consists of 16 bits followed by data that can be of variable lengths in multiples of 8 bits. If the device is configured with CSB tied low, framing begins with the first rising edge of SCLK.

The instruction phase is the first 16 bits transmitted. As shown in the following figure, the instruction phase is divided into a number of bit fields.

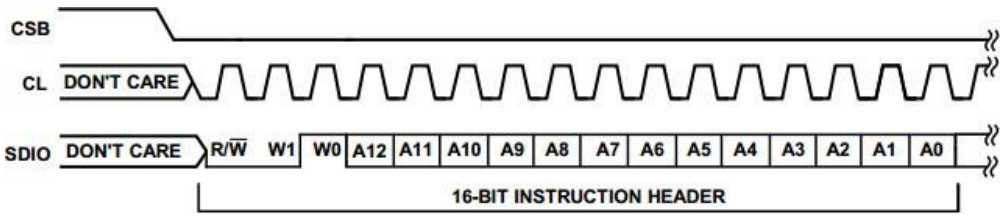


Figure 3.2.1. Instruction Phase bit field

The first bit in the stream is the read/write indicator bit (R/W). When this bit is high, a read is being requested, otherwise indicates it is a write operation.

W1 and W0 represent the number of data bytes to transfer for either read or write as shown in the following table(W1 and W0 setting table). If the number of bytes to transfer is three or less (00, 01, or 10), CSB can stall high on byte boundaries. Stalling on a non-byte boundary terminates the communications cycle. If these bits are 11, data can be transferred until CSB transitions high. CSB is not allowed to stall during the streaming process.

Table 8. W1 and W0 settings

W1:W0	Action	CSB stalling
00	1 byte of data can be transferred.	Optional
01	2 bytes of data can be transferred.	Optional
10	3 bytes of data can be transferred.	Optional
11	4 or more bytes of data can be transferred. CSB must be held low for entire sequence; otherwise, the cycle is terminated.	No

Data follows the instruction phase. The amount of data sent is determined by the word length (Bit W0 and Bit W1). This can be one or more bytes of data. All data is composed of 8-bit words.
Data can be sent in either MSB-first mode or LSB-first mode (by setting 'LSB_first' bit). On power up, MSB-first mode is the default. This can be changed by programming the configuration register. In MSB-first mode, the serial exchange starts with the highest-order bit and ends with the LSB. In LSB-first mode, the order is reversed. The detail is shown in the below figure.

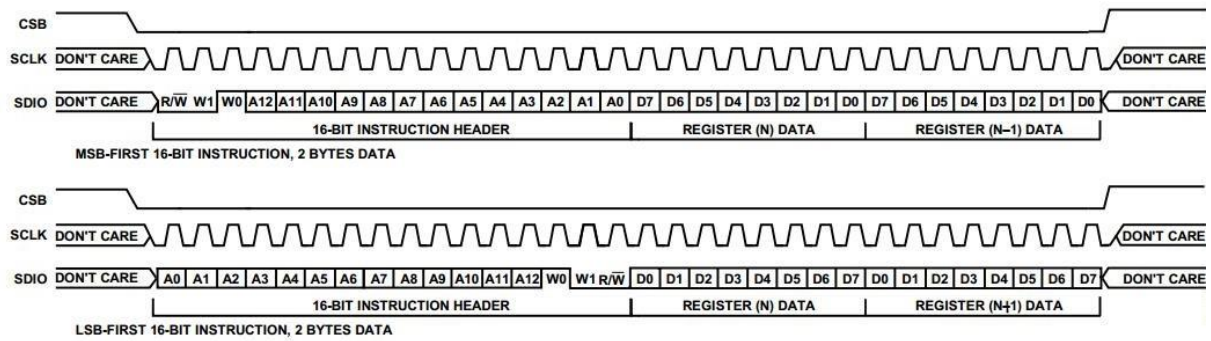


Figure 3.2.2. MSB First and LSB First Instruction and data Phases

Register bit 'SDO_active' is responsible for activating SDO on devices. If this bit is cleared, then SDO is inactive and read data is routed to the SDI pin. If this bit is set, read data is placed on the SDO pin. The default for this bit is low, making SDO inactive.

3.2.2. I2C operation

I2C bus uses SCL and SDA as signal lines. Both lines are connected to VDDIO externally via pull-up resistors so that they are pulled high when the bus is free. The I2C device address of SSA-L163FD is shown below. The LSB bit of the 7bits device address is configured via SA0 pin.

Table 9. I2C Address

SAD6	SAD5	SAD4	SAD3	SAD2	SAD1	SAD0	W/R
0	1	0	0	1	1	SAO	0/1

Table 10. SAD+Read/Write patterns

Command	SAD[6:1]	SAD[0]=SA0	R/W	SAD+R/W
Read	010011	0	1	01001101(4dh)
Write	010011	0	0	01001100(4ch)
Read	010011	1	1	01001111(4fh)
Write	010011	1	0	01001110(4eh)

The I2C interface protocol has special bus signal conditions. Start (S), stop (P) and binary data conditions are shown below. At start condition, SCL is high and SDA has a falling edge. Then the slave address is sent. After the 7 address bits, the direction control bit R/W selects the read or write operation. When a slave device recognizes that it is being addressed, it should acknowledge by pulling SDA low in the ninth SCL (ACK) cycle.

At stop condition, SCL is also high, but SDA has a rising edge. Data must be held stable at SDA when SCL is high. Data can change value at SDA only when SCL is low.

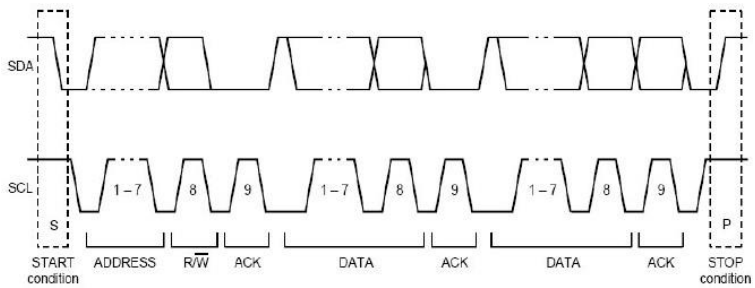


Figure 3.2.2. I2C Protocol

Table 11. Transfer when master is writing one byte to slave

Master	S	SAD+W		SUB		DATA		P
Slave			SAK		SAK		SAK	

Table 12. Transfer when master is writing multiple bytes to slave

Master	S	SAD+W		SUB		DATA		DATA		P
Slave			SAK		SAK		SAK		SAK	

Table 13. Transfer when master is receiving one byte of data from slave

Master	S	SAD+W		SUB		SR	SAD+R			NMASK	P
Slave			SAK		SAK			SAK	DATA		

Table 14. Transfer when master is receiving multiple bytes to data from slave

Master	S	SAD+W		SUB		SR	SAD+R			MAK		MAK		NMASK	P
Slave			SAK		SAK			SAK	DATA		DATA		DATA		

Note:

Symbol	Symbol explain	Symbol	Symbol explain
SAD	slave address	SAK	slave acknowledge
W	write	MAK	master acknowledge
R	read	NMASK	no master acknowledge
S	start	SUB	Sub-address(register address)
P	stop	DATA	Read or write data
SR	start		

4. Terminology and functionally

4.1. Terminology

4.1.1. Sensitivity

Sensitivity describes the gain of the sensor and can be determined e.g. by applying 1g acceleration to it. As the sensor can measure DC accelerations this can be done easily by pointing the axis of interest towards the center of the earth, noting the output value, rotating the sensor by 180 degrees (pointing to the sky) and noting the output value again. By doing so, ±1 g acceleration is applied to the sensor. Subtract the larger output value from the smaller one, and dividing the result by 2, leads to the actual sensitivity of the sensor. This value changes very little over temperature and also time. The sensitivity tolerance describes the range of sensitivities of a large population of sensors.

4.1.2. Zero-g level

Zero-g level offset (TyOff) describes the deviation of an actual output signal from the ideal output signal if no acceleration is present. A sensor in a steady state on a horizontal surface measure 0 g in X axis and 0 g in Y axis whereas the Z axis measure 1g. The output is ideally in the middle of the dynamic range of the sensor (content of output data registers are 00h, data expressed as 2's complement number). A deviation from ideal value in this case is called Zero-g offset. Offset is to some extent a result of stress to MEMS sensor and therefore the offset can slightly change after mounting the sensor onto a printed circuit board or exposing it to extensive mechanical stress. Offset changes little over temperature; see "Zero-g level change vs. temperature". The Zero-g level tolerance (TyOff) describes the standard deviation of the range of Zero-g levels of a population of sensors.

4.2. Functionality

4.2.1. Power mode

The SSA-L163FD has three different power modes. Besides normal mode, which represents the fully operational state of the device, there are two special energy saving modes: low-power mode and suspend mode.

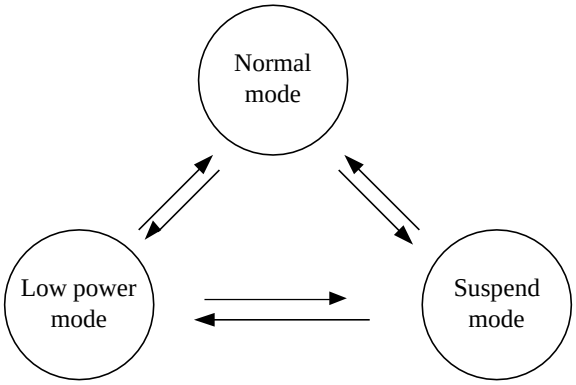


Figure 4.2.1. Power mode

In normal mode, all parts of the electronic circuit are held powered-up and data acquisition is performed continuously.

In suspend mode, the whole analog part, including the oscillator, Ana LDO, Dig LDO and Drive Buffer are all powered down, no data acquisition is performed and the only supported operation is to read/write the registers. Suspend mode is entered by writing '11' or '10' to the (0x11) 'pwr_mode' bits.

In low power mode, the device is periodically switching between a sleep phase and a wake-up phase. The wake-up phase essentially corresponding to operation in normal mode with complete power-up of the circuitry. During the sleep phase the analog part except the oscillator is powered down.

During the wake-up phase, if a enabled interrupt is detected, the device stays in the wake-up phase as long as the interrupt condition endures (non-latched interrupt), or until the latch time expires (temporary interrupt), or until the interrupt is reset (latched interrupt). If no interrupt detected, the device enters the sleep phase.

4.2.2. Sensor data

The width of acceleration data is 14bits given in two's complement representation. The 14bits for each axis are split into an MSB part (one byte containing bits 13 to 6) and an LSB lower part (one byte containing bits 5 to 0)

4.2.3. Factory calibration

The IC is factory calibrated for sensitivity (So) and Zero-g level (TyOff). The trimming values are stored inside the chip's nonvolatile memory. The trimming parameters are loaded to registers while SSA-L163FD reset (POR or software reset). This allows using the device without further calibration.

4.3. Interrupt controller

Interrupt engines are integrated in the SSA-L163FD. Each interrupt can be independently enabled and configured. If the condition of an enabled interrupt is fulfilled, the corresponding status bit is set to 1 and the selected interrupt pin is activated. There are two interrupt pins, INT1 and INT2; interrupts can be freely mapped to any of these two pins. The pin state is a logic 'or' combination of all mapped interrupts.

4.3.1. General features

An interrupt is cleared depending on the selected interrupt mode, which is common to all interrupts. There are three different interrupt modes: non-latched, latched and temporary. The mode is selected by the 'latch_int' bits according to the following table.

Table 15. Interrupt mode selection

latch_int1/2	Interrupt mode
0000	non-latched
0001	temporary latched 250ms
0010	temporary latched 500ms
0011	temporary latched 1s
0100	temporary latched 2s
0101	temporary latched 4s
0110	temporary latched 8s
0111	latched
1000	non-latched
1001	temporary latched 1ms
1010	temporary latched 1ms
1011	temporary latched 2ms
1100	temporary latched 25ms
1101	temporary latched 50ms
1110	temporary latched 100ms
1111	latched

An interrupt is generated if its activation condition is met. It can't be cleared as long as the activation condition is fulfilled. In the non-latched mode the interrupt status bit and the selected pin (INT1 or INT2) are cleared as soon as the activation condition is no more valid. Exceptions to this behavior are the new data and orientation, which are automatically reset after a fixed time.

In the latched mode an asserted interrupt status and the selected pin are cleared by writing 1 to (0x20) 'reset_int' bit. If the activation condition still holds when it is cleared, the interrupt status is asserted again with the next change of the acceleration registers.

In the temporary mode an asserted interrupt and selected pin are cleared after a defined period of time. The behavior of the different interrupt modes is shown in the following figure.

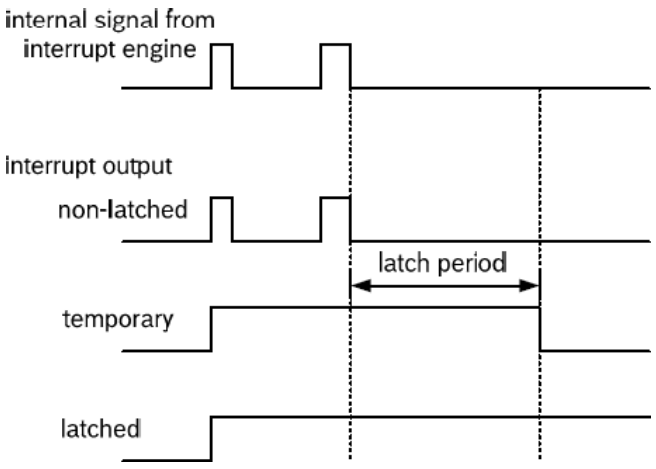


Figure 4.3.1. Interrupt mode

4.3.2. Mapping

The mapping of interrupts to the interrupt pins is done by registers 'INT_MAP' (0x19 0x1a and 0x1b), setting int1_inttype (e.g. int1_freefall) to 1 can map this type of interrupt to INT1 pin and setting int2_inttyp to 1 can map this type interrupt to INT2 pin.

4.3.3. Electrical behavior (INT1/INT2 to open-drive or push-pull)

Both interrupt pins can be configured to show desired electrical behavior. The active level for each pin is set by register bit int1_lvl (int2_lvl), if int1_lvl (int2_lvl) = 0 (1), then the pin INT1 (INT2) is 0 (1) active.

Also the electric type of the interrupt pin can be selected. By setting int1_od (int2_od) = 1 (0), the interrupt pin output type can be set to be open-drive (push-pull).

4.3.4. New data interrupt

This interrupt serves for synchronous reading of acceleration data. It is generated after an acceleration data was calculated. The interrupt is cleared automatically before the next acceleration data is ready.

4.3.5. Active detection

Active detection uses the slope between successive acceleration signals to detect changes in motion. An interrupt is generated when the slope (absolute value of acceleration difference) exceeds a preset threshold. The threshold is set with the value of 28H register with the LSB corresponding to 255LSB of acceleration data, that is 3.9mg in 2g-range, 7.8mg in 4g-range, 15.6mg in 8g-range and 31.3mg in 16g-range. And the maximum value is 1g in 2g-range, 2g in 4g-range, 4g in 8g-range and 8g in 16g-range.

The time difference between the successive acceleration signals depends is fixed to 1ms.

Active detection can be enabled (disabled) for each axis separately by writing '1' to bits 'active_int_en_x/y/z'. The active interrupt is generated if the slope of any of the enabled axes exceeds the threshold for ['active_dur'+1] consecutive times. As soon as the slopes of all enabled axes fall below this threshold for ['active_dur'+1] consecutive times, the interrupt is cleared unless the interrupt signal is latched.

The interrupt status is stored in the (0x09) 'active_int' bit. The (0x0b) bit 'active_first_x/y/z' records which axis triggered the active interrupt first and the sign of this acceleration data that triggered the interrupt is recorded in the (0x0b) bit 'active_sign'.

4.3.6. Tap detection

Tap detection has a functional similarity with a common laptop touch-pad or clicking keys of a computer mouse. A tap event is detected if a pre-defined pattern of the acceleration slope is fulfilled at least for one axis. Two different tap events are distinguished: A single tap is a single event within a certain time, followed by a certain quiet time. A double tap consist a first such event followed by a second event within a defined time.

Single tap interrupt is enabled by writing 1 to the (0x16) 's_tap_int_en' bit and double tap interrupt is enabled by writing 1 to the (0x16) 'd_tap_int_en' bit. The status of the single tap interrupt is stored in the (0x09) 's_tap_int' bit and the status of the double tap interrupt is stored in the (0x09) 'd_tap_int' bit.

The slope threshold for detecting a tap event is set by the (0x2b) "tap_th" bits with the LSB corresponding to 31LSB of acceleration data that is 62.5mg in 2g-range, 125mg in 4g-range, 250mg in 8g-range, 500mg in 16g-range. And the maximum value equals to the full scale in each range.

The following figure meaning of different timing parameter is visualized.

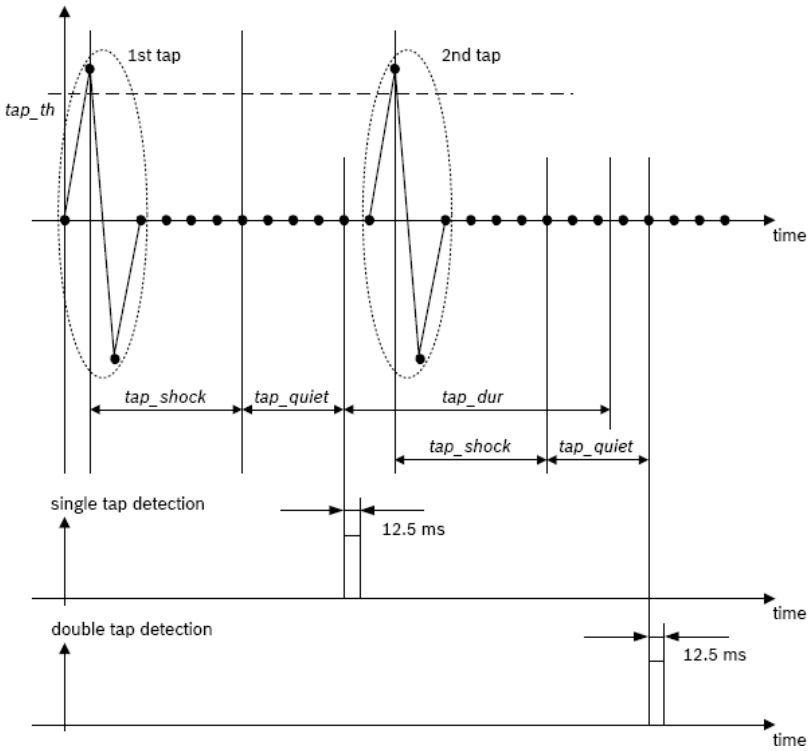


Figure 4.3.6. Timing of tap detection

The parameter ‘tap_shock’ and ‘tap_quiet’ apply to both single and double tap detection, while ‘tap_dur’ applies to double detection only. Within the duration of ‘tap_shock’ any slope exceeding ‘tap_th’ after the first event is ignored, within the duration of ‘tap_quiet’ there must be no slope exceeding ‘tap_th’, otherwise the first event will be cancelled.

A single tap is detected and the single tap interrupt is generated after the combination durations of ‘tap_shock’ and ‘tap_quiet’, if the corresponding slope conditions are fulfilled. The interrupt is cleared after a delay of 12.5ms in non-latched mode.

A double tap is detected and the double tap interrupt is generated if an event fulfilling the conditions for a single tap occurs within the set duration in ‘tap_dur’ after the completion of the first tap event. The interrupt is cleared after a delay in non-latched mode.

The sign of the slope of the first tap which triggered the interrupt is stored in the (0x0b) ‘tap_sign’ bit (0 means positive, 1 means negative). The axis which triggered the interrupt is indicated by the (0x0b) ‘tap_first_x/y/z’ bit.

Note: ‘tap_shock’ ‘tap_quiet’ ‘tap_dur’ ‘tap_th’ can be set by modifying register 0x2a and 0x2b

4.3.7. Orientation recognition

The orientation recognition feature informs on an orientation change of sensor with respect to the gravitation field vector 'g'. The measured acceleration vector components with respect to the gravitation field are defined as shown in the following figure.

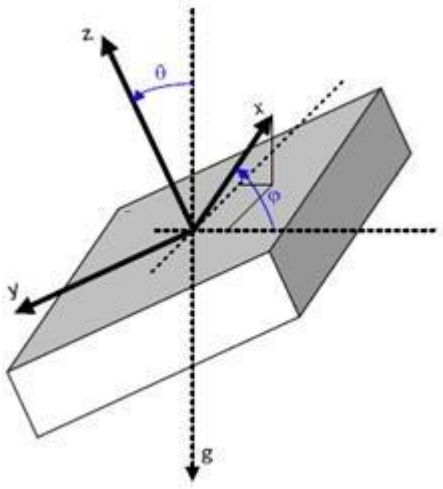


Figure 4.3.7. Definition of vector components

Therefore, the magnitudes of the acceleration vectors are calculated as follows:

$$acc_x = lg\sin(\theta) * \cos(\varphi)$$
$$acc_y = -\lg\sin(\theta) * \sin(\varphi)$$
$$acc_z = \lg\cos(\theta)$$

Depending on the magnitudes of the acceleration vectors the orientation of the device in the space is determined and stored in the (0x09) 'orient_int' bit. There are three orientation calculation modes with different thresholds for switching between different orientations: symmetrical, high-asymmetrical and low-asymmetrical. The mode is selected by setting the (0x2c) 'orient_mode' bit. For each orientation mode, the 'orient' bits have a different meaning as show in the following tables.

Table 16. Meaning of "orient" bits in symmetric mode

Orient	Name	Angle	Condition
X00	Portrait upright	$315^o < \varphi < 45^o$	|acc_y| < |acc_x| - 'hyst' & acc_x>= 0
X01	Portrait upside down	$135^o < \varphi < 225^o$	|acc_y| < |acc_x| - 'hyst' & acc_x< 0
X10	Landscape left	$45^o < \varphi < 135^o$	|acc_y| >= |acc_x| + 'hyst' & acc_y < 0
X11	Landscape right	$225^o < \varphi < 315^o$	|acc_y| >= |acc_x| + 'hyst' & acc_y >= 0

Table 17. Meaning of "orient" bits in high-asymmetric mode

Orient	Name	Angle	Condition
X00	Portrait upright	$297^o < \varphi < 63^o$	|acc_y| < 2*|acc_x| - 'hyst' &acc_x>= 0
X01	Portrait upside down	$117^o < \varphi < 243^o$	|acc_y| < 2*|acc_x| - 'hyst' &acc_x< 0
X10	Landscape left	$63^o < \varphi < 117^o$	|acc_y| >= 2*|acc_x| + 'hyst' & acc_y < 0
X11	Landscape right	$243^o < \varphi < 297^o$	|acc_y| >= 2*|acc_x| + 'hyst' & acc_y >= 0

Table 18. Meaning of "orient" bits in low-asymmetric mode

Orient	Name	Angle	Condition
X00	Portrait upright	$333^o < \varphi < 27^o$	|acc_y| < 0.5*|acc_x| - 'hyst' &acc_x>= 0
X01	Portrait upside down	$153^o < \varphi < 207^o$	|acc_y| < 0.5*|acc_x| - 'hyst' &acc_x< 0
X10	Landscape left	$27^o < \varphi < 153^o$	|acc_y| >= 0.5*|acc_x| + 'hyst' & acc_y < 0
X11	Landscape right	$207^o < \varphi < 333^o$	|acc_y| >= 0.5*|acc_x| + 'hyst' & acc_y >= 0

In the preceding tables, the parameter 'hyst' stands for a hysteresis which can be selected by the (0x2c) 'orient_hyst' bit. 1LSB of 'orient_hyst' always corresponds to 62.5mg in any g-range. The MSB of 'orient' bits contains information about the direction of the z-axis. It is set to 0(1) if acc_z>=0 (acc_z<0). The hysteresis for z axis is fixed to 0.2g.

The orient interrupt is enabled by writing the (0x16) 'orient_int_en' bit. The interrupt is generated if the value of 'orient' has changed. It is automatically cleared after one stable period of the orient value in non-latched mode. In temporary latched or latched mode, the orient value is kept fixed as long as the interrupt persists. After cleaning the interrupt, the 'orient' will updated with the next following value change.

The change of the 'orient' value and the generation of the interrupt can be blocked according to conditions selected by setting the value of the (0x2c) 'orient_block' bit as described by the following table.

Table 19. Blocking conditions for orientation recognition

Orient_block	Conditions
00b	No blocking
01b	Z blocking
10b	Z blocking or acceleration slope in any axis > 0.2g
11b	No blocking

The Z blocking is defined by the following inequality :

$$|acc\_z| > z\_blocking$$

The parameter z_blocking of the above given equation stands for the contents of the (0x2d) 'z_blocking' bit. Hereby it is possible to define a blocking value between 0g and 0.9375g with an LSB = 0.0625g.

4.3.8 Freefall interrupt

This interrupt is based on the comparison of acceleration data against a low-g threshold. The interrupt is enabled by writing 1 to the (0x17) 'freefall_int_en' bit. There are two modes available: single mode and sum mode. In single mode the acceleration of each axis is compared with the threshold. In sum mode, the sum of absolute values of all accelerations |acc_x| + |acc_y| + |acc_z| is compared with the threshold. The mode is selected by the (0x24) 'freefall_mode' bit. The free fall threshold is set through the (0x23) 'freefall_th' bits with 1 LSB corresponding to an acceleration of 7.81mg. A hysteresis can be selected by setting the (0x24) 'freefall_hy' bits with 1 LSB corresponding to 125mg.

The freefall interrupt is generated if the absolute values of the acceleration of all axes or their sum are lower than the threshold for at least the time defined by the (0x22) 'freefall_dur' bits. The interrupt is reset if the absolute value of at least one axis or the sum is higher than the threshold plus the hysteresis for at least one data acquisition. The interrupt status is stored in the (0x09) 'freefall_int' bit.

5. Application hints

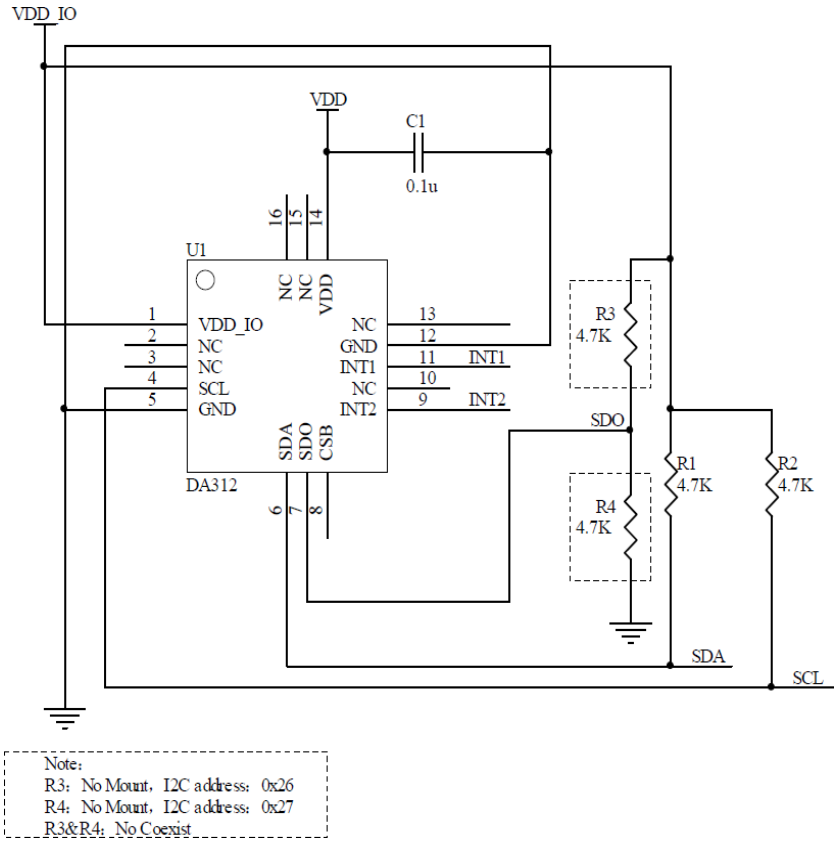


Figure 5.1. SSA-L163FD I2C electrical connect

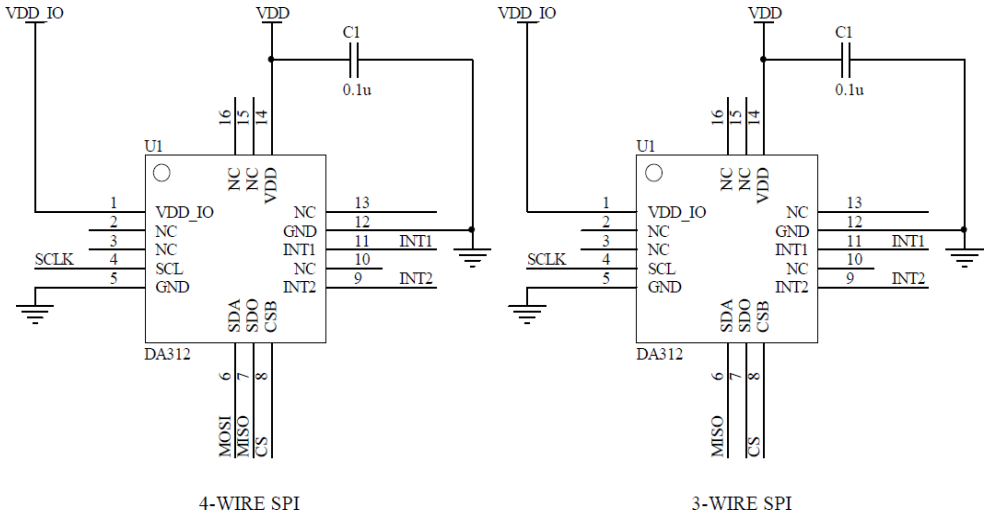


Figure 5.2. SSA-L163FD SPI electrical connect

The device core is supplied through Vdd line while the I/O pads are supplied through Vdd_IO line. Power supply decoupling capacitors (100 nF ceramic) should be placed as near as possible to the pin 14 of the device (common design practice).

The functionality of the device and the measured acceleration data is selectable and accessible through the I2C or SPI interfaces. When using the I2C, CS must be tied high or keep NC (not connect). The functions, the threshold and the timing of the two interrupt pins (INT1 and INT2) can be completely programmed by the user through the I2C/SPI interface.

6. Register mapping

The table given below provides a listing of the 8 bit registers embedded in the device and the related addresses:

Table 20. Register address map

Name	Type	Register address	Default	Soft Reset
SPI_CONFIG	RW	0x00	00H	NO
CHIPID	R	0x01	13H	NO
ACC_X_LSB	R	0x02	00H	NO
ACC_X_MSB	R	0x03	00H	NO
ACC_Y_LSB	R	0x04	00H	NO
ACC_Y_MSB	R	0x05	00H	NO
ACC_Z_LSB	R	0x06	00H	NO
ACC_Z_MSB	R	0x07	00H	NO
MOTION_FLAG	R	0x09	00H	NO
NEWDATA_FLAG	R	0x0A	00H	NO
TAP_ACTIVE_STATUS	R	0x0B	00H	NO
ORIENT_STATUS	R	0x0C	00H	NO
RESOLUTION_RANGE	RW	0x0F	00H	YES
ODR_AXIS	RW	0x10	0FH	YES
MODE_BW	RW	0x11	9EH	YES
SWAP_POLARITY	RW	0x12	01H	YES
INT_SET1	RW	0x16	00H	YES
INT_SET2	RW	0x17	00H	YES
INT_MAP1	RW	0x19	00H	YES
INT_MAP2	RW	0x1A	00H	YES
INT_MAP3	RW	0x1B	00H	YES
INT_CONFIG	RW	0x20	05H	YES
INT_LATCH	RW	0x21	00H	YES
FREEFALL_DUR	RW	0x22	09H	YES
FREEFALL_THS	RW	0x23	30H	YES
FREEFALL_HYST	RW	0x24	01H	YES
ACTIVE_DUR	RW	0x27	00H	YES
ACTIVE_THS	RW	0x28	14H	YES
TAP_DUR	RW	0x2A	04H	YES
TAP_THS	RW	0x2B	0AH	YES
ORIENT_HYST	RW	0x2C	18H	YES
Z_BLOCK	RW	0x2D	08H	YES

7. Registers description

7.1. SPI_CONFIG(00H)

Table 21. SPI_CONFIG register
Default data: 0x00 Type: RW

SDO Active	LSB First	Soft Reset	Unused	Unused	Soft Reset	LSB First	SDO Active

Table 22. SPI_CONFIG description

SDO Active	0:3-wire SPI 1:4-wire SPI
LSB First	0:MSB First 1:LSB First
Soft Reset	1: soft reset

7.2. CHIPID (01h)

Table 23. CHIPID register
Default data: 0x13 Type: R

0	0	0	1	0	0	1	1

7.3. ACC_X_LSB (02H), ACC_X_MSB (03H)

X-axis acceleration data, the value is expressed in two complement byte and are left justified.

Table 24. ACC_X_LSB register
Default data: 0x00 Type: R

D[5]	D[4]	D[3]	D[2]	D[1]	D[0]		

Table 25. ACC_X_MSB register
Default data: 0x00 Type: R

D[13]	D[12]	D[11]	D[10]	D[9]	D[8]	D[7]	D[6]

7.4. ACC_Y_LSB (04H), ACC_Y_MSB (05H)

Y-axis acceleration data, the value is expressed in two complement byte and are left justified.

Table 26.ACC_Y_LSB register
Default data: 0x00 Type: R

D[5]	D[4]	D[3]	D[2]	D[1]	D[0]		

Table 27.ACC_Y_MSB register
Default data: 0x00 Type: R

D[13]	D[12]	D[11]	D[10]	D[9]	D[8]	D[7]	D[6]

7.5. ACC_Z_LSB (06H), ACC_Z_MSB (07H)

Z-axis acceleration data, the value is expressed in two complement byte and are left justified.

Table 28.ACC_Z_LSB register
Default data: 0x00 Type: R

D[5]	D[4]	D[3]	D[2]	D[1]	D[0]		

Table 29.ACC_Z_MSB register
Default data: 0x00 Type: R

D[13]	D[12]	D[11]	D[10]	D[9]	D[8]	D[7]	D[6]

7.6. MOTION_FLAG (09H)

Table 30.MOTION_FLAG register
Default data: 0x00 Type: R

	orient_int	s_tap_int	d_tap_int		active_int		freefall_int

Table 31. MOTION_FLAG register description

orient_int	0:no orient interrupt 1:orient interrupt has occurred
s_tap_int	0:no single tap interrupt 1: single tap interrupt has occurred
d_tap_int	0:no double tap interrupt 1: double tap interrupt has occurred
active_int	0:no active interrupt 1: active interrupt has occurred
freefall_int	0:no freefall interrupt 1: freefall interrupt has occurred

7.7. NEWDATA_FLAG (0AH)

Table 32. NEWDATA_FLAG register
Default data: 0x00 Type: R

							new_data_int

Table 33. NEWDATA_FLAG register description

new_data_int	0: no new_data interrupt 1: new_data interrupt has occurred

7.8. TAP_ACTIVE_STATUS register (0BH)

Table 34.TAP_ACTIVE_STATUS register
Default data: 0x00 Type: R

tap_sign	tap_first_x	tap_first_y	tap_first_z	active_sign	active_first_x	active_first_y	active_first_z

Table 35. TAP_ACTIVE_STATUS register description

tap_sign	Sign of the first tap that triggered interrupt 0: positive 1: negative
tap_first_x	0: X is not the triggering axis of the tap interrupt 1: indicate X is the triggering axis of the tap interrupt.
tap_first_y	0: Y is not the triggering axis of the tap interrupt 1: indicate Y is the triggering axis of the tap interrupt.
tap_first_z	0: Z is not the triggering axis of the tap interrupt 1: indicate Z is the triggering axis of the tap interrupt.
active_sign	active_sign: Sign of the 1st active interrupt. 0: positive, 1: negative
active_first_x	0: X is not the triggering axis of the active interrupt 1: indicate X is the triggering axis of the active interrupt.
active_first_y	0: Y is not the triggering axis of the active interrupt 1: indicate Y is the triggering axis of the active interrupt.
active_first_z	0: Z is not the triggering axis of the active interrupt 1: indicate Z is the triggering axis of the active interrupt.

7.9. ORIENT_STATUS register (0CH)

Table 36.ORIENT_STATUS register
Default data: 0x00 Type: R

	orient[2]	orient[1]	orient[0]				

37.ORIENT_STATUS register description

Orient[2]	orientation value of 'z' axis 0: upward looking, 1: downward looking
Orient[1:0]	orientation value of 'x', 'y' axes; 00: portrait upright ; 01: portrait upside down; 10: landscape left ; 11:landscape right

7.10. RESOLUTION_RANGE (0FH)

Table 38. RESOLUTION_RANGE register
Default data: 0x00 Type:RW

HP_en				resolution[1]	resolution[0]	fs[1]	fs[0]

Table 39. RESOLUTION_RANGE register description

HP_en	0:disable high pass filter 1:enable
resolution[1:0]	00:14bit 01:12bit 10:10bit 11:8bit
fs[1:0]	full scale 00: +/-2g 01: +/-4g 10:+/-8g 11:+/-16g

7.11. ODR_AXIS (10H)

Table 40. ODR_AXIS register
Default data: 0x0F Type:RW

X-axis_disable	Y-axis_disable	Z-axis_disable		ODR[3]	ODR[2]	ODR[1]	ODR[0]

41. ODR_AXIS register description
Default data: 0x0F Type:RW

x-axis_disable	0: enable X axis; 1: disable X axis
y-axis_disable	0: enable Y axis; 1: disable Y axis
z-axis_disable	0: enable Z axis; 1: disable Z axis
ODR[3:0]	0000: 1Hz (not available in normal mode) ; 0001: 1.95Hz (not available in normal mode) 0010: 3.9Hz ; 0011: 7.81Hz; 0100: 15.63Hz; 0101: 31.25Hz; 0110: 62.5Hz 0111: 125Hz; 1000: 250Hz; 1001: 500Hz (not available in low power mode); 1010: 1000Hz (not available in low power mode); 1011-1111: 1000Hz (not available in low power mode)

7.12. MODE_BW register

Table 42. MODE_BW register
Default data: 0x9E Type:RW

pwr_mode [1]	pwr_mode [0]		low_power_bw [3]	low_power_bw [2]	low_power_bw[1]	low_power_bw[0]	

Table 43. MODE_BW register description

pwr_mode[1:0]	00: normal mode, 01: low power mode, 1x: suspend mode.
low_power_bw [3:0]	0000-0010: 1.95Hz 0011: 3.9Hz 0100: 7.81Hz 0101: 15.63Hz 0110: 31.25Hz 0111: 62.5Hz 1000: 125Hz 1001: 250Hz 1010: 500Hz 1011-1111: 500Hz

7.13. SWAP_POLARITY (12H)

Table 44. SWAP_POLARITY register
Default data: 0x01 Type:RW
Swap & Polarity register is OTP register too, OTP address: 0x13

				X_polarity	Y_polarity	Z_polarity	X_Y_swap

Table 45. SWAP_POLARITY register description

X_polarity	0: remain the polarity of X-axis. 1: reverse the polarity of X-axis.
Y_polarity	0: remain the polarity of Y-axis. 1: reverse the polarity of Y-axis.
Z_polarity	0: remain the polarity of Z-axis. 1: reverse the polarity of Z-axis.
X_Y_swap	0: Don't need swap the output data for X/Y axis 1: swap the output data for X/Y axis.

7.14. INT_SET1 register (16H)

Table 46. INT_SET1 register
Default data: 0x00 Type:RW

INT_source	orient_int_en	s_tap_int_en	d_tap_int_en		active_int_en_z	active_int_en_y	active_int_en_x

Table 47. INT_SET1 register description

INT_source	0:unfiltered data 1:filtered data(ODR)
orient_int_en	0: disable the orient interrupt. 1: enable the orient interrupt.
s_tap_int_en	0: disable the single tap interrupt. 1: enable the single tap interrupt.
d_tap_int_en	0: disable the double tap interrupt. 1: enable the double tap interrupt.
active_int_en_z	0: disable the active interrupt for the z axis. 1: enable the active interrupt for the z axis.
active_int_en_y	0: disable the active interrupt for the y axis. 1: enable the active interrupt for the y axis.
active_int_en_x	0: disable the active interrupt for the x axis. 1: enable the active interrupt for the x axis.

7.15. INT_SET2 register (17H)

Table 48. INT_SET2 register
Default data: 0x00 Type:RW

			new_data_int_en	freefall_int_en			

Table 49. INT_SET2 register

new_data_int_en	0: disable the new data interrupt. 1: enable the new data interrupt.
freefall_int_en	0: disable the freefall interrupt. 1: enable the freefall interrupt

7.16. INT_MAP1 register (19H)

Table 50. INT_MAP1 register
Default data: 0x00 Type:RW

	int1_orient	int1_s_tap	int1_d_tap		int1_active		int1_freefall

Table 51. INT_MAP1 register description

int1_orient	0: doesn't mapping orient interrupt to INT1 1: mapping orient interrupt to INT1
int1_s_tap	0: doesn't mapping single tap interrupt to INT1 1: mapping single tap interrupt to INT1
int1_d_tap	0: doesn't mapping double tap interrupt to INT1 1: mapping double tap interrupt to INT1
int1_active	0: doesn't mapping active interrupt to INT1 1: mapping active interrupt to INT1
int1_freefall	0: doesn't mapping freefall interrupt to INT1 1: mapping freefall interrupt to INT1

7.17. INT_MAP2 register (1AH)

Table 52. INT_MAP1 register
Default data: 0x00 Type:RW

int2_new_data								int1_new_data

Table 53. INT_MAP2 register description

int2_new_data	0: doesn't mapping new data interrupt to INT2 1: mapping new data interrupt to INT2
int1_new_data	0: doesn't mapping new data interrupt to INT1 1: mapping new data interrupt to INT1

7.18. INT_MAP3 register (1BH)

Table 54. INT_MAP3 register
Default data: 0x00 Type:RW

	int2_orient	int2_s_tap	int2_d_tap		int2_active		int2_freefall

Table 55. INT_MAP3 register description
Default data: 0x00 Type:RW

int2_orient	int2_X: "1"mapping interrupt X to INT2
int2_s_tap	
int2_d_tap	
int2_active	
int2_freefall	

7.19. INT_CONFIG register (20H)

Table 56. INT_CONFIG register
Default data: 0x05 Type:RW

Reset_int				int2_od	int2_lvl	int1_od	int1_lvl

Table 57. INT_CONFIG register description

Reset_int	Write'1'to reset all latched int.
Int2_od	0: select push-pull output for INT2 1: selects OD output for INT2
Int2_lvl	0: selects active level low for pin INT2 1: selects active level high for pin INT2
int1_od	0: select push-pull output for INT1 1: selects OD output for INT1
int1_lvl	0: selects active level low for pin INT1 1: selects active level high for pin INT1

7.20. INT_LATCH (21H)

Table 58. INT_LATCH register
Default data: 0x00 Type:RW

latch_int2[3]	latch_int2[2]	latch_int2[1]	latch_int2[0]	latch_int1[3]	latch_int1[2]	latch_int1[1]	latch_int1[0]

Table 59. INT_LATCH register description

latch_int2[3:0]	0000: non-latched; 0001: temporary latched 250ms 0010: temporary latched 500ms 0011: temporary latched 1s 0100: temporary latched 2s 0101: temporary latched 4s 0110: temporary latched 8s 0111: latched; 1000: non-latched; 1001: temporary latched 1ms 1010: temporary latched 1ms; 1011: temporary latched 2ms; 1100: temporary latched 25ms 1101: temporary latched 50ms; 1110: temporary latched 100ms ; 1111: latched
latch_int1[3:0]	0000: non-latched; 0001: temporary latched 250ms 0010: temporary latched 500ms; 0011: temporary latched 1s; 0100: temporary latched 2s; 0101: temporary latched 4s; 0110: temporary latched 8s; 0111: latched; 1000: non-latched; 1001: temporary latched 1ms; 1010: temporary latched 1ms; 1011: temporary latched 2ms; 1100: temporary latched 25ms; 1101: temporary latched 50ms; 1110: temporary latched 100ms; 1111: latched

7.21. FREEFALL_DUR (22H)

Table 60. IFREEFALL_DUR register
Default data: 0x09 Type:RW

freefall_dur[7]	freefall_dur[6]	freefall_dur[5]	freefall_dur[4]	freefall_dur [3]	freefall_dur [2]	freefall_dur [1]	freefall_dur [0]

Table 61. IFREEFALL_DUR register description

freefall_dur[7:0]	Delay time for freefall delay_time = (freefall_dur + 1) * 2ms range from 2ms to 512ms default: 20ms

7.22. FREEFALL_THS (23H)

Table 62. FREEFALL_THS register
Default data: 0x30 Type:RW

freefall_th[7]	freefall_th [6]	freefall_th [5]	freefall_th[4]	freefall_th [3]	freefall_th [2]	freefall_th [1]	freefall_th [0]

Table 63. FREEFALL_THS register description

freefall_th[7:0]	freefall threshold = freefall_th * 7.81mg LSB = 7.81mg default is 375mg

7.23. FREEFALL_HYST (24H)

Table 63. FREEFALL_HYST register
Default data: 0x01 Type:RW

					freefall_mode	freefall_hy[1]	freefall_hy[0]

Table 64. FREEFALL_HYST register description

freefall_mode	0: single mode. 1: sum mode.
freefall_hy[1:0]	Set the hysteresis for freefall detection. Free fall hysteresis time = freefall_hy* 125mg LSB = 125mg

7.24 ACTIVE_DUR register

Table 66. ACTIVE_DUR register
Default data: 0x00 Type:RW

						active_dur[1]	active_dur[0]

Table 67. ACTIVE_DUR register

active_dur[1:0]	Active duration time = (active_dur + 1) ms

7.25 ACTIVE_THS (28H)

Table 68. ACTIVE_THS register
Default data: 0x14 Type:RW

active_th[7]	active_th [6]	active_th [5]	active_th[4]	active_th [3]	active_th [2]	active_th [1]	active_th [0]

Table 69. ACTIVE_THS register description

active_th[7:0]	Threshold of active interrupt=Active_th*K(mg) ; K = 3.91(2g range), K =7.81(4g range), K=15.625(8g range), K=31.25(16g range).

7.26 TAP_DUR (2AH)

Table 70. TAP_DUR register
Default data: 0x04 Type:RW

tap_quiet	tap_shock				tap_dur[2]	tap_dur[1]	tap_dur[0]

Table 71. TAP_DUR register description
Default data: 0x01 Type:RW

tap_quiet	0: tap quiet duration 30ms. 1: tap quiet duration 20ms.
tap_shock	0: tap shock duration 50ms. 1: tap shock duration 70ms.
tap_dur[2:0]	Tap duration selects the length of the time window for the second shock. 000: 50ms 001: 100ms 010: 150ms 011: 200ms 100: 250ms 101: 375ms 110: 500ms 111: 700ms

7.27. TAP_THS register (2BH)

Table 72. TAP_THS register
Default data: 0x0a Type:RW

			tap_th [4]	tap_th [3]	tap_th [2]	tap_th [1]	tap_th [0]

Table 73. TAP_THS register description

tap_th [4:0]	Threshold of tap interrupt=Tap_th*K(mg) ; K = 62.5(2g range); K = 125(4g range) ; K = 250(8g range) K = 500 (16g range)

7.28. ORIENT_HYST (2CH)

Table 74. ORIENT_HYST register
Default data: 0x18 Type:RW

	orient_hyst[2]	orient_hyst[1]	orient_hyst[0]	orient_block[1]	orient_block [0]	orient_mode [1]	orient_mode [0]

Table 75. ORIENT_HYST register description

orient_hyst[2:0]	Set the hysteresis of the orientation interrupt; 1LSB = 62.5mg.
orient_block[1:0]	00: no blocking; 01: z blocking; 10: z blocking or slope in any axis > 0.2g; 11: no blocking
orient_mode [1:0]	00: symmetrical; 01: high-asymmetrical; 10: low-asymmetrical; 11:synmmetrical

7.29. Z_BLOCK (2DH)

Table 76. Z_BLOCK register
Default data: 0x08 Type:RW

				z_blocking[3]	z_blocking[2]	z_blocking[1]	z_blocking[0]

Table 77. Z_BLOCK register description

z_blocking[3:0]	Defines the blocking acc_z between 0g to 0.9375g. 1LSB=62.5mg

8. Mechanical dimension

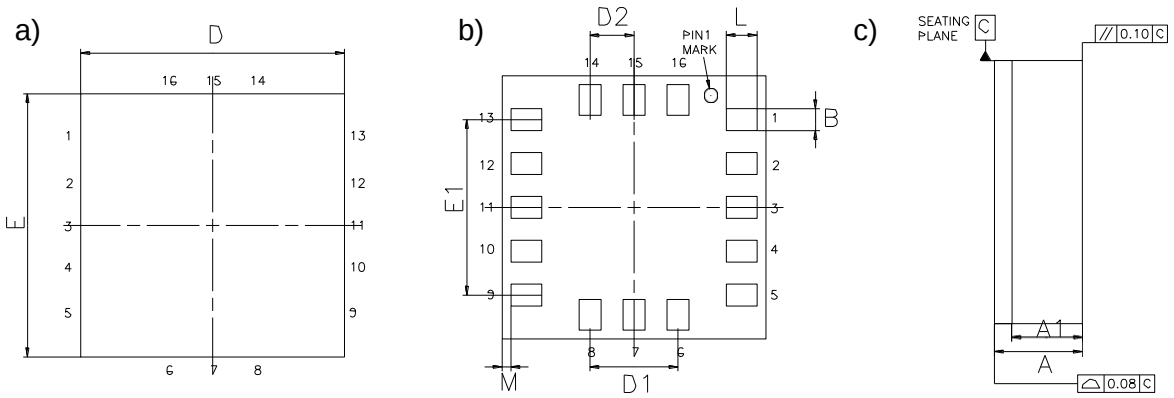


Figure 8.1. a) Top view; b) Bottom view; c) Side view

Table 78. Dimensions

SYMBOL	DIMENSION (MM)		
	MIN.	NOM.	MAX.
A	0.84	0.92	1.00
A1	0.68	0.73	0.78
B	0.20	0.25	0.30
D	2.90	3.00	3.10
D1	0.90	1.00	1.10
D2	0.50 NOM.		
E	2.90	3.00	3.10
E1	1.90	2.00	2.10
L	0.30	0.35	0.40
M	0.04	0.10	0.16

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