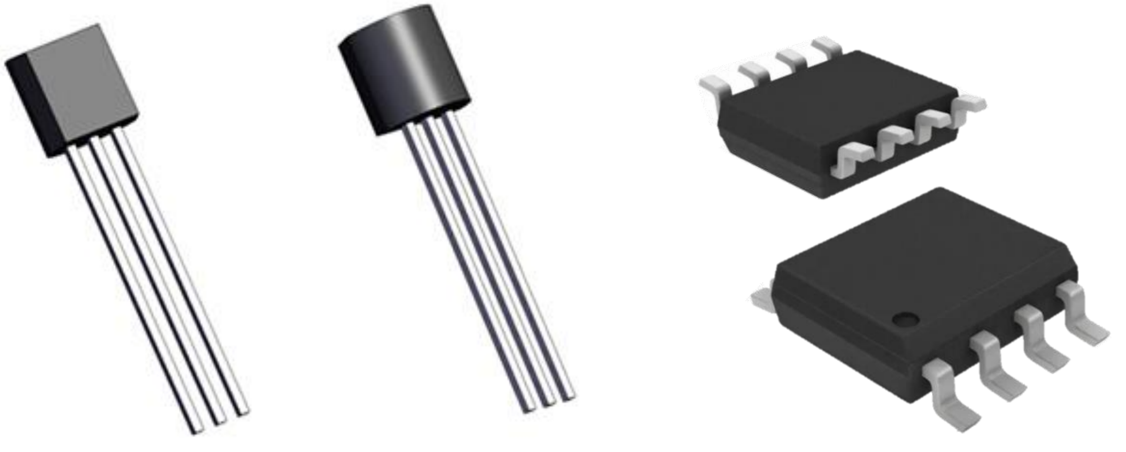
SST-DM10

Programmable resolution 1-wire digital thermometer



PRODUCTS FEATURES

- Unique 64-Bit Serial Code Stored in an On-Board ROM
- Multidrop Capability Simplifies Distributed Temperature-Sensing Applications
- Requires No External Components
- Can Be Powered from Data Line; Power Supply Range is 2.5V to 5.5V
- ±0.4°C Accuracy from -10°C to +70°C
- Thermometer Resolution is User Selectable from 9 to 12 Bits
- User-Definable Nonvolatile Alarm Settings
- 1-Wire Interface Requires Only One Port Pin for

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1. DC electrical characteristics

Parameter	Symbol	Conditions	Min.	TYP	MAX	Units
Supply Voltage	V_{DD}	Local power (Note 1)	+3		+5.5	V
Pullup supply voltage	V_{PU}	Parasite power (Notes 1,2)	+3		+5.5	V
		Local power (Notes 1,2)	+3		V_{DD}	
Thermometer error	t_{ERR}	-10~+85˚C (Note 3)			±0.5	˚C
		-30~+100˚C (Note 3)			±1	
		-55~+125˚C (Note 3)			±2	
Input Logic-Low	V_{IL}	(Notes 1, 4, 5)	-0.3		+0.8	V
Input Logic-High	V_{IH}	Local power (Notes 1,6)	+2.2	The lower of 5.5 or V_{DD} +0.3		V
		Parasite power (Notes 1,6)	+3.3			
Sink current	I_L	$V_{I/O}$ = 0.4 V	4			mA
Standby Current	I_{DDS}	(Notes 7, 8)		750	1000	nA
Active current	I_{DD}	V_{DD} = 5V (Note 9)		1	1.5	mA
DQ input current	I_{DQ}	(Note 10)		5		μA
Drift		(Note 11)		±0.2		˚C

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Absolute maximum ratings	
Voltage range on any pin relative to ground	-0.5V to +6.0V
Operating temperature range	-55~+125˚C
Storage temperature range	-55~+125˚C

AC electrical characteristics -NV memory						
parameter	**symbol**	**conditions**	**Min**	**TYP**	**Max**	**Units**
NV White cycle time	t_{WR}			2	10	ms
EEPROM writes	N_{EEWR}	-55~+55˚C	50k			Writes
EEPROM data retention	t_{EEDR}	-55~+55˚C	10			years

AC electrical characteristics							
parameter	**symbol**	**conditions**		**Min**	**TYP**	**Max**	**Units**
Temperature conversion time	t_{CONV}	9-bit resolution	(Note 12)			93.7	ms
		10-bit resolution				185.5	
		11-bit resolution				375	
		12-bit resolution				750	
Time to strong pullup on	t_{SPON}	Start convert T command issued				10	μs
Time slot	t_{SLOT}	(Note 12)		60		120	μs
Recovery time	t_{REC}	(Note 12)		1			μs

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AC electrical characteristics						
parameter	symbol	conditions	Min	TYP	Max	Units
Write 0 low time	t_{LOW0}	(Note 12)	60		120	µs
Write 1 low time	t_{LOW1}	(Note 12)	1		15	µs
Read data valid	t_{RDV}	(Note 12)			15	µs
Reset time high	t_{RSTH}	(Note 12)	480			µs
Reset time low	t_{RSTL}	(Note 12, 13)	480			µs
Presence-detect high	t_{PDHIGH}	(Note 12)	15		60	µs
Presence-detect high	t_{PDLOW}	(Note 12)	60		240	µs
Capacitance	$C_{IN/OUT}$				25	pF

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Note	Description
1	All voltages are referenced to ground.
2	The Pullup Supply Voltage specification assumes that the pullup device is ideal, and therefore the high level of the pullup is equal to V_{PU}. In order to meet the V_{IH} spec of the SST-PPM, the actual supply rail for the strong pullup transistor must include margin for the voltage drop across the transistor when it is turned on; thus: $V_{PU\_ACTUAL} = V_{PU\_IDEAL} + V_{TRANSISTOR}$.
3	See typical performance curve in **graph of the thermometer error dependence on the temperature**
4	Logic-low voltages are specified at a sink current of 4mA
5	To guarantee a presence pulse under low voltage parasite power conditions, V_{ILMAX} may have to be reduced to as low as 0.5V.
6	Logic-high voltages are specified at a source current of 1mA.
7	Standby current specified up to +70°C. Standby current typically is 3µA at +125°C.
8	To minimize I_{DDS}, DQ should be within the following ranges: GND ≤ DQ ≤ GND + 0.3V or V_{DD} – 0.3V ≤ DQ ≤ V_{DD}.
9	Active current refers to supply current during active temperature conversions or EEPROM writes.
10	DQ line is high (“high-Z” state).
11	Drift data is based on a 1000-hour stress test at +125°C with V_{DD} = 5.5V.
12	See the **timing diagrams**
13	Under parasite power, if t_{RSTL} > 960 µs, a power-on reset can occur

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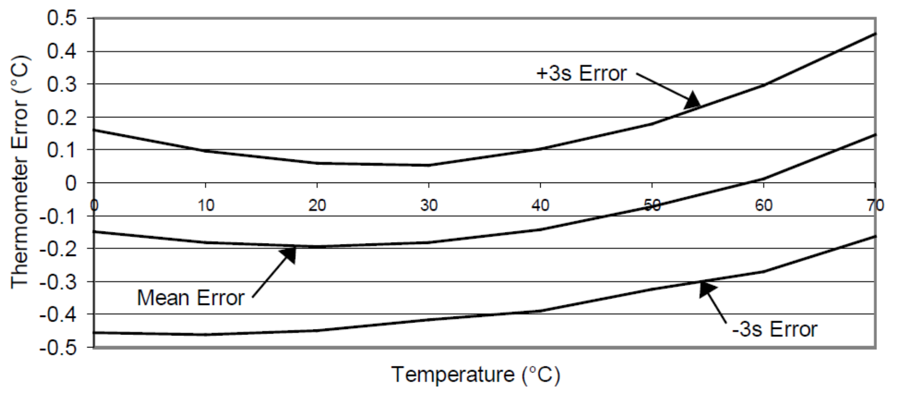
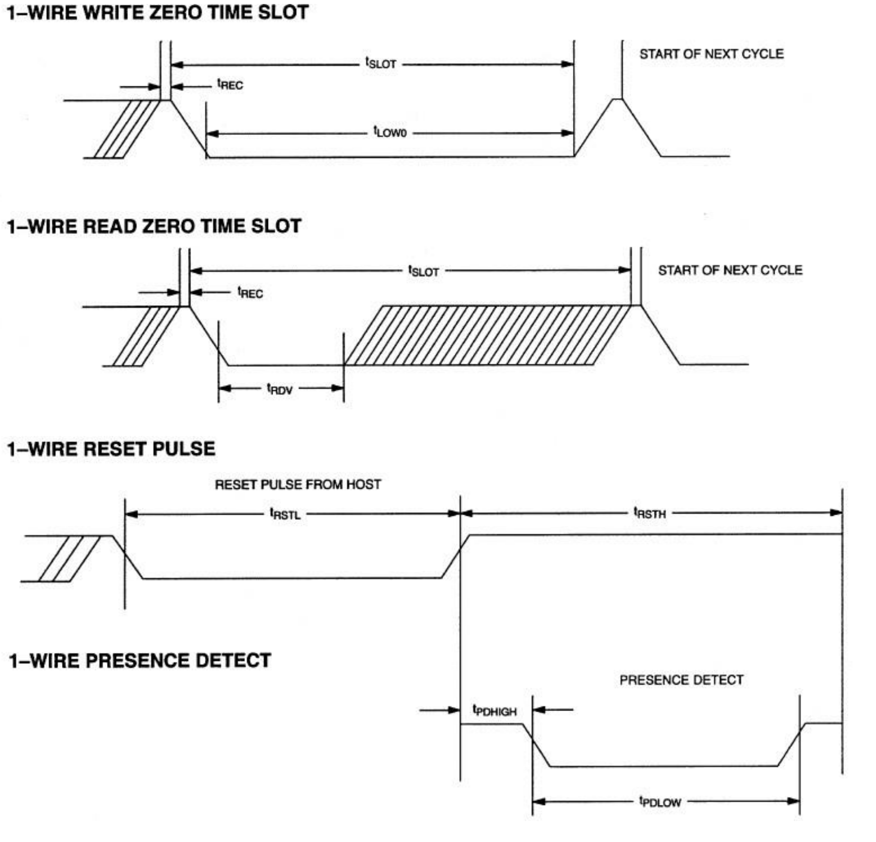
Graph of the thermometer error dependence on the temperature:



Timing diagrams :



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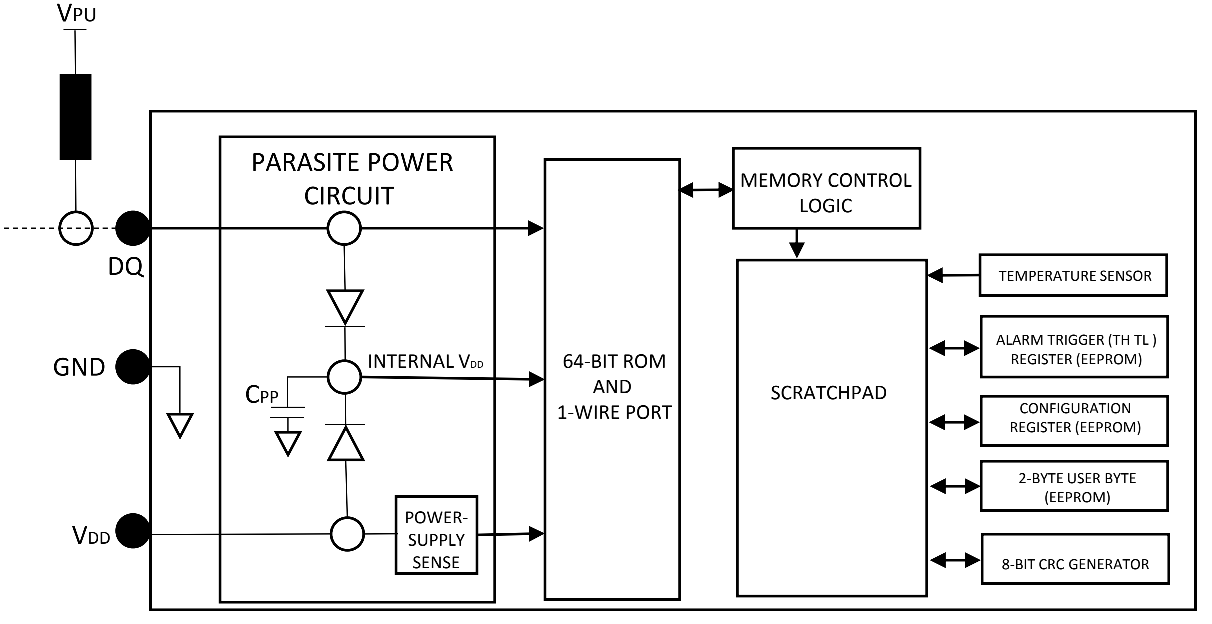
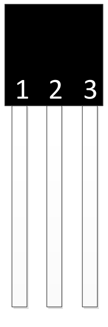
2. Block diagram





Pins	Parameter	Definition
3	V_{DD}	Optional V_{DD}. V_{DD} must be grounted for operation in parasite power mode
2	DQ	Data input/output. Open-drain 1-Wire interface pin. Also provides power to the device when used in parasite power mode (see the Powering the SST-PPxxx section.)
1	GND	Ground

*** Descriptions of other package options - slide 27**

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Overview

The 64-bit ROM stores the device's unique serial code. The scratchpad memory contains the 2-byte temperature register that stores the digital output from the temperature sensor. In addition, the scratchpad provides access to the 1-byte upper and lower alarm trigger registers (TH and TL) and the 1-byte configuration register. The configuration register allows the user to set the resolution of the temperature- to-digital conversion to 9, 10, 11, or 12 bits. And there are 2-byte user programmable EEPROM. The TH, TL, configuration registers, and 2-byte user programmable EEPROM are nonvolatile (EEPROM), so they will retain data when the device is powered down.

The SST-DM10 uses 1-Wire bus protocol that implements bus communication using one control signal. The control line requires a weak pullup resistor since device are linked to the bus via a 3-state or open-drain port (the DQ pin in the case of the SST-DM10). In this bus system, the microprocessor (the master device) identifies and addresses devices on the bus using each device's unique 64-bit code. Because each device has a unique code, the number of devices that can be addressed on one bus is virtually unlimited. The 1-Wire bus protocol, including detailed explanations of the commands and "time slots," is covered in the 1-Wire Bus System section.

Another feature of the SST-DM10 is the ability to operate without an external power supply. Power is instead supplied through the 1-Wire pullup resistor via the DQ pin when the bus is high. The high bus signal also charges an internal capacitor (CPP), which then supplies power to the device when the bus is low. This method of deriving power from the 1-Wire bus is referred to as "parasite power." As an alternative, the SST-DM10 may also be powered by an external supply on VDD.

Operation—measuring temperature

The core functionality of the SST-DM10 is its direct-to-digital temperature sensor. The resolution of the temperature sensor is user-configurable to 9, 10, 11, or 12 bits, corresponding to increments of 0.5°C, 0.25°C, 0.125°C, and 0.0625°C, respectively. The default resolution at power-up is 12-bit. The SST-DM10 powers up in a low-power idle state. To initiate a temperature measurement and A-to-D conversion, the master must issue a Convert T [44h] command. Following the conversion, the resulting thermal data is stored in the 2-byte temperature register in the scratchpad memory and the SST-DM10 returns to its idle state. If the SST-DM10 is powered by an external supply, the master can issue "read time slots" (see the 1-Wire Bus System section) after the Convert T command and the SST-DM10 will respond by transmitting 0 while the temperature conversion is in progress and 1 when the conversion is done. If the SST-DM10 is powered with parasite power, this notification technique cannot be used since the bus must be pulled high by a strong pullup during the entire temperature conversion. The bus requirements for parasite power are explained in detail in the Powering the SST-DM10 section.

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The SST-DM10 output temperature data is calibrated in degrees Celsius; for Fahrenheit applications, a lookup table or conversion routine must be used. The temperature data is stored as a 16-bit sign-extended two's complement number in the temperature register:

BIT	7	6	5	4	3	2	1	0
LS BYTE	2^3	2^2	2	2^0	2^{-1}	2^{-2}	2^{-3}	2^{-4}

BIT	15	14	13	12	11	10	9	8
MS BYTE	S	S	S	S	S	2^6	2^5	2^4

The sign bits (S) indicate if the temperature is positive or negative: for positive numbers S = 0 and for negative numbers S = 1. If the SST-DM10 is configured for 12-bit resolution, all bits in the temperature register will contain valid data. For 11-bit resolution, bit 0 is undefined. For 10-bit resolution, bits 1 and 0 are undefined, and for 9-bit resolution bits 2, 1, and 0 are undefined. Table 1 gives examples of digital output data and the corresponding temperature reading for 12-bit resolution conversions.

TEMPERATURE (°C)	DIGITAL OUTPUT (BINARY)	DIGITAL OUTPUT (HEX)
+125	0000 0111 1101 0000	07D0h
+85*	0000 0101 0101 0000	0550h
+25.0625	0000 0001 1001 0001	0191h
+10.125	0000 0000 1010 0010	00A2h
+0.5	0000 0000 0000 1000	0008h
0	0000 0000 0000 0000	0000h
-0.5	1111 1111 1111 1000	FFF8h
-10.125	1111 1111 0101 1110	FF5Eh
-25.0625	1111 1110 0110 1111	FE6Fh
-55	1111 1100 1001 0000	FC90h

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Operation—alarm signaling

After the SST-DM10 performs a temperature conversion, the temperature value is compared to the user- defined two's complement alarm trigger values stored in the 1-byte TH and TL registers:

BIT	7	6	5	4	3	2	1	0
LS BYTE	S	2^6	2^5	2^4	2^3	2^2	2^1	2^0

The sign bit (S) indicates if the value is positive or negative: for positive numbers S = 0 and for negative numbers S = 1. The TH and TL registers are nonvolatile (EEPROM) so they will retain data when the device is powered down. TH and TL can be accessed through bytes 2 and 3 of the scratchpad as explained in the Memory section.

Only bits 11 through 4 of the temperature register are used in the T_H and T_L comparison since T_H and T_L are 8-bit registers. If the measured temperature is lower than or equal to T_L or higher than or equal to T_H, an alarm condition exists and an alarm flag is set inside the SST-DM10. This flag is updated after every temperature measurement; therefore, if the alarm condition goes away, the flag will be turned off after the next temperature conversion. The master device can check the alarm flag status of all SST-DM10s on the bus by issuing an Alarm Search command. Any SST-DM10s with a set alarm flag will respond to the command, so the master can determine exactly which SST-DM10s have experienced an alarm condition. If an alarm condition exists and the T_H or T_L settings have changed, another temperature conversion should be done to validate the alarm condition.

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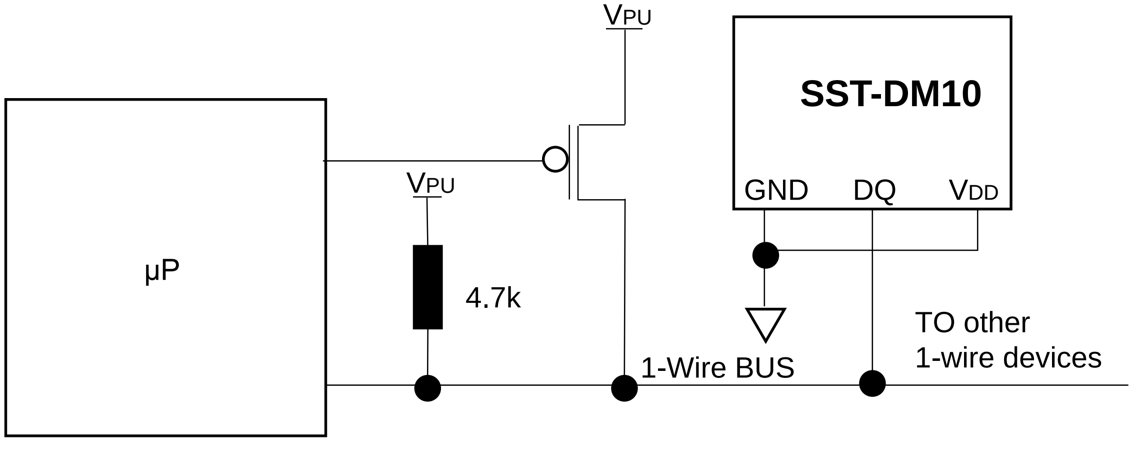
Powering the SST-DM10

The SST-DM10 can be powered by an external supply on the VDD pin, or it can operate in “parasite power” mode, which allows the SST-DM10 to function without a local external supply. Parasite power is very useful for applications that require remote temperature sensing or that are very space constrained. Block diagram 2 shows the SST-DM10’s parasite-power control circuitry, which “steals” power from the 1-Wire bus via the DQ pin when the bus is high. The stolen charge powers the SST-DM10 while the bus is high, and some of the charge is stored on the parasite power capacitor (CPP) to provide power when the bus is low. When the SST-DM10 is used in parasite power mode, the VDD pin must be connected to ground.

In parasite power mode, the 1-Wire bus and C_{PP} can provide sufficient current to the SST-DM10 for most operations as long as the specified timing and voltage requirements are met (see the *DC Electrical Characteristics* and *AC Electrical Characteristics*). However, when the SST-DM10 is performing temperature conversions or copying data from the scratchpad memory to EEPROM, the operating current can be as high as 1.5mA. This current can cause an unacceptable voltage drop across the weak 1-Wire pullup resistor and is more current than can be supplied by C_{PP}. To assure that the SST-DM10 has sufficient supply current, it is necessary to provide a strong pullup on the 1-Wire bus whenever temperature conversions are taking place or data is being copied from the scratchpad to EEPROM. This can be accomplished by using a MOSFET to pull the bus directly to the rail as shown below. The 1-Wire bus must be switched to the strong pullup within 10µs (max) after a Convert T [44h] or Copy Scratchpad [48h] command is issued, and the bus must be held high by the pullup for the duration of the conversion (t_{CONV}) or data transfer (t_{WR} = 10ms). No other activity can take place on the 1-Wire bus while the pullup is enabled.



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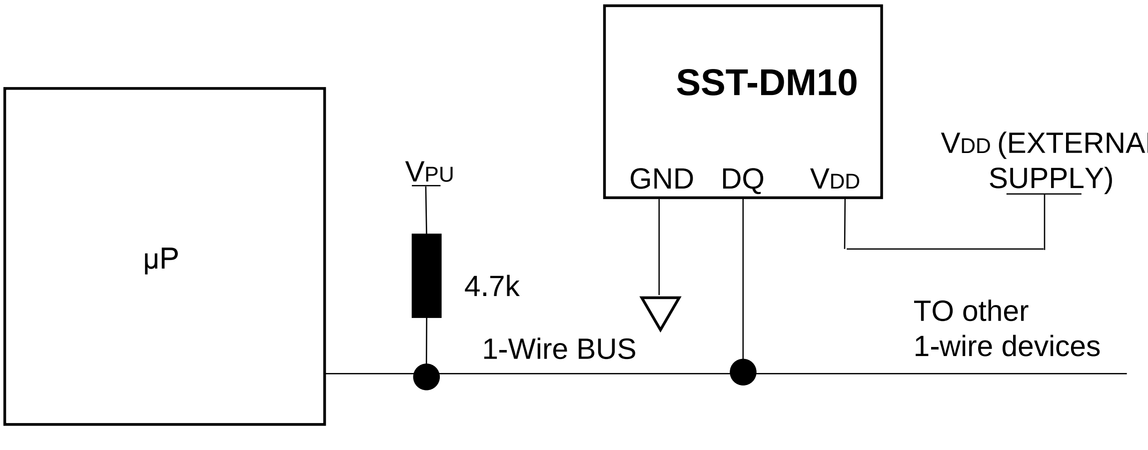
The SST-DM10 can also be powered by the conventional method of connecting an external power supply to the V_{DD} pin, as shown below. The advantage of this method is that the MOSFET pullup is not required, and the 1-Wire bus is free to carry other traffic during the temperature conversion time.
The use of parasite power is not recommended for temperatures above +100°C since the SST-DM10 may not be able to sustain communications due to the higher leakage currents that can exist at these temperatures. For applications in which such temperatures are likely, it is strongly recommended that the SST-DM10 be powered by an external power supply.

In some situations the bus master may not know whether the SST-DM10s on the bus are parasite powered or powered by external supplies. The master needs this information to determine if the strong bus pullup should be used during temperature conversions. To get this information, the master can issue a Skip ROM [CCh] command followed by a Read Power Supply [B4h] command followed by a "read time slot". During the read time slot, parasite powered SST-DM10s will pull the bus low, and externally powered SST-DM10 will let the bus remain high. If the bus is pulled low, the master knows that it must supply the strong pullup on the 1-Wire bus during temperature conversions.



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Each SST-DM10 contains a unique 64–bit code stored in ROM. The least significant 8 bits of the ROM code contain the SST-DM10 1-Wire family code: 28h. The next 48 bits contain a unique serial number. The most significant 8 bits contain a cyclic redundancy check (CRC) byte that is calculated from the first 56 bits of the ROM code.

8-BIT CRC		48-BIT SERIAL NUMBER		8-BIT FAMILY CODE (28h)	
MSB	LSB	MSB	LSB	MSB	LSB

Memory

The SST-DM10 memory is organized as shown in table below. The memory consists of an SRAM scratchpad with nonvolatile EEPROM storage for the high and low alarm trigger registers (TH and TL) , configuration register, and 2-byte user programmable EEPROM. Note that if the SST-DM10 alarm function is not used, the TH and TL registers can serve as general-purpose memory.

BYTE 0	Temperature LSB (50 h)	85 °C
BYTE 1	Temperature MSB (05h)	
BYTE 2	TH Register or user byte 1*	
BYTE 3	TL Register or user byte 2*	
BYTE 4	Configuration register*	
BYTE 5	Reserved (FFh)	
BYTE 6	User byte 3	
BYTE 7	User byte 4	
BYTE 8	CRC*	

EEPROM
TH Register or user byte 1
TL Register or user byte 2
Configuration register
User byte 3
User byte 4

Byte 0 and byte 1 of the scratchpad contain the LSB and the MSB of the temperature register, respectively. These bytes are read-only. Bytes 2 and 3 provide access to TH and TL registers. Byte 4 contains the configuration register data, which is explained in detail in the Configuration Register section.

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Byte 5 is reserved for internal use by the device and cannot be overwritten. Bytes 6, and 7 are for User. Byte 8 of the scratchpad is read-only and contains the CRC code for bytes 0 through 7 of the scratchpad. The SST-DM10 generates this CRC using the method described in the CRC Generation section.

Data is written to bytes 2, 3, 4, 6, and 7 of the scratchpad using the Write Scratchpad [4Eh] command; the data must be transmitted to the SST-DM10 starting with the least significant bit of byte 2. To verify data integrity, the scratchpad can be read (using the Read Scratchpad [BEh] command) after the data is written. When reading the scratchpad, data is transferred over the 1-Wire bus starting with the least significant bit of byte 0. To transfer the TH, TL and configuration data from the scratchpad to EEPROM, the master must issue the Copy Scratchpad [48h] command.

Data in the EEPROM registers is retained when the device is powered down; at power-up the EEPROM data is reloaded into the corresponding scratchpad locations. Data can also be reloaded from EEPROM to the scratchpad at any time using the Recall E2 [B8h] command. The master can issue read time slots following the Recall E2 command and the SST-DM10 will indicate the status of the recall by transmitting 0 while the recall is in progress and 1 when the recall is done.

Configuration register

Byte 4 of the scratchpad memory contains the configuration register, which is organized as illustrated below. `

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0	R1	R0	1	1	1	1	1

The user can set the conversion resolution of the SST-DM10 using the R0 and R1 bits in this register as shown below. The power-up default of these bits is R0 = 1 and R1 = 1 (12-bit resolution). Note that there is a direct tradeoff between resolution and conversion time. Bit 7 and bits 0 to 4 in the configuration register are reserved for internal use by the device and cannot be overwritten.

R1	R0	Resolution (BITS)	MAX conversion time	
0	0	9	93.75ms	(t_{CONV}/8)
0	1	10	187.5ms	(t_{CONV}/4)
1	0	11	375ms	(t_{CONV}/2)
1	1	12	750ms	(t_{CONV})

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CRC GENERATION

CRC bytes are provided as part of the SST-DM10's 64-bit ROM code and in the 9th byte of the scratchpad memory. The ROM code CRC is calculated from the first 56 bits of the ROM code and is contained in the most significant byte of the ROM. The scratchpad CRC is calculated from the data stored in the scratchpad, and therefore it changes when the data in the scratchpad changes. The CRCs provide the bus

master with a method of data validation when data is read from the SST-DM10. To verify that data has been read correctly, the bus master must re-calculate the CRC from the received data and then compare

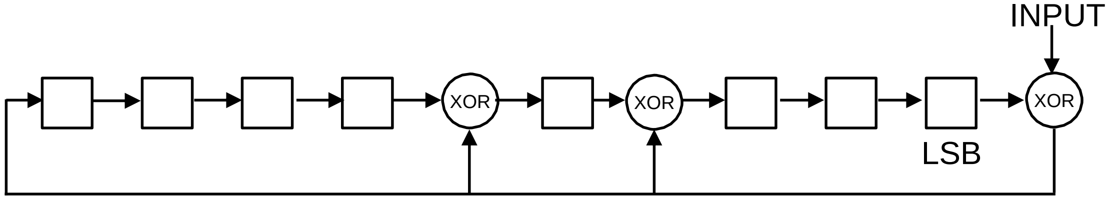
this value to either the ROM code CRC (for ROM reads) or to the scratchpad CRC (for scratchpad reads). If the calculated CRC matches the read CRC, the data has been received error free. The comparison of CRC values and the decision to continue with an operation are determined entirely by the bus master. There

is no circuitry inside the SST-DM10 that prevents a command sequence from proceeding if the SST-DM10 CRC (ROM or scratchpad) does not match the value generated by the bus master.

The equivalent polynomial function of the CRC (ROM or scratchpad) is:

$$CRC = X^8 + X^5 + X^4 + 1$$

The bus master can re-calculate the CRC and compare it to the CRC values from the GX18B20 using the polynomial generator shown below.



This circuit consists of a shift register and XOR gates, and the shift register bits are initialized to 0. Starting with the least significant bit of the ROM code or the least significant bit of byte 0 in the scratchpad, one bit at a time should shifted into the shift register. After shifting in the 56th bit from the ROM or the most significant bit of byte 7 from the scratchpad, the polynomial generator will contain the re-calculated CRC. Next, the 8-bit ROM code or scratchpad CRC from the SST-DM10 must be shifted into the circuit. At this point, if the re-calculated CRC was correct, the shift register will contain all 0s.

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1-WIRE BUS SYSTEM

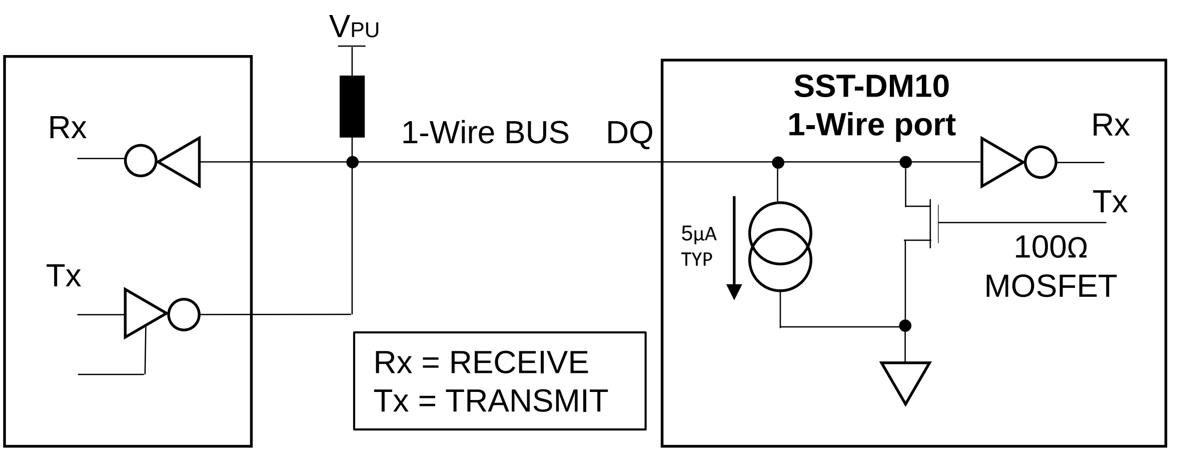
The 1-Wire bus system uses a single bus master to control one or more slave devices. The SST-DM10 is always a slave. When there is only one slave on the bus, the system is referred to as a “single-drop” system; the system is “multidrop” if there are multiple slaves on the bus.

All data and commands are transmitted least significant bit first over the 1-Wire bus.

The following discussion of the 1-Wire bus system is broken down into three topics: hardware configuration, transaction sequence, and 1-Wire signaling (signal types and timing).

HARDWARE CONFIGURATION

The 1-Wire bus has by definition only a single data line. Each device (master or slave) interfaces to the data line via an open-drain or 3-state port. This allows each device to “release” the data line when the device is not transmitting data so the bus is available for use by another device. The 1-Wire port of the SST-DM10 (the DQ pin) is open drain with an internal circuit equivalent to that shown in Figure below.



The 1-Wire bus requires an external pullup resistor of approximately 5kΩ; thus, the idle state for the 1-Wire bus is high. If for any reason a transaction needs to be suspended, the bus MUST be left in the idle state if the transaction is to resume. Infinite recovery time can occur between bits so long as the 1-Wire bus is in the inactive (high) state during the recovery period. If the bus is held low for more than 1ms, all components on the bus will be reset.

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TRANSACTION SEQUENCE

The transaction sequence for accessing the SST-DM10 is as follows:

Step 1. Initialization

Step 2. ROM Command (followed by any required data exchange)

Step 3. SST-DM10 Function Command (followed by any required data exchange)

It is very important to follow this sequence every time the SST-DM10 is accessed, as the SST-DM10 will not respond if any steps in the sequence are missing or out of order. Exceptions to this rule are the Search ROM [F0h] and Alarm Search [ECh] commands. After issuing either of these ROM commands, the master must return to Step 1 in the sequence.

INITIALIZATION

All transactions on the 1-Wire bus begin with an initialization sequence. The initialization sequence consists of a reset pulse transmitted by the bus master followed by presence pulse(s) transmitted by the slave(s). The presence pulse lets the bus master know that slave devices (such as the SST-DM10) are on the bus and are ready to operate. Timing for the reset and presence pulses is detailed in the 1-Wire Signaling section.

ROM COMMANDS

After the bus master has detected a presence pulse, it can issue a ROM command. These commands operate on the unique 64-bit ROM codes of each slave device and allow the master to single out a specific device if many are present on the 1-Wire bus. These commands also allow the master to determine how many and what types of devices are present on the bus or if any device has experienced an alarm condition. There are five ROM commands, and each command is 8 bits long. The master device must issue an appropriate ROM command before issuing a SST-DM10 function command. A flowchart for operation of the ROM commands is shown in slide 21.

SEARCH ROM [F0h]

When a system is initially powered up, the master must identify the ROM codes of all slave devices on the bus, which allows the master to determine the number of slaves and their device types. The master learns the ROM codes through a process of elimination that requires the master to perform a Search ROM cycle (i.e., Search ROM command followed by data exchange) as many times as necessary to identify all of the slave devices. If there is only one slave on the bus, the simpler Read ROM command (see below) can be used in place of the Search ROM process. After every Search ROM cycle, the bus master must return to Step 1 (Initialization) in the transaction sequence.

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READ ROM [33h]

This command can only be used when there is one slave on the bus. It allows the bus master to read the slave's 64-bit ROM code without using the Search ROM procedure. If this command is used when there is more than one slave present on the bus, a data collision will occur when all the slaves attempt to respond at the same time.

MATCH ROM [55h]

The match ROM command followed by a 64-bit ROM code sequence allows the bus master to address a specific slave device on a multidrop or single-drop bus. Only the slave that exactly matches the 64-bit ROM code sequence will respond to the function command issued by the master; all other slaves on the bus will wait for a reset pulse.

SKIP ROM [CCh]

The master can use this command to address all devices on the bus simultaneously without sending out any ROM code information. For example, the master can make all SST-DM10s on the bus perform simultaneous temperature conversions by issuing a Skip ROM command followed by a Convert T [44h] command.

Note that the Read Scratchpad [BEh] command can follow the Skip ROM command only if there is a single slave device on the bus. In this case, time is saved by allowing the master to read from the slave without sending the device's 64-bit ROM code. A Skip ROM command followed by a Read Scratchpad command will cause a data collision on the bus if there is more than one slave since multiple devices will attempt to transmit data simultaneously.

ALARM SEARCH [ECh]

The operation of this command is identical to the operation of the Search ROM command except that only slaves with a set alarm flag will respond. This command allows the master device to determine if
any SST-DM10s experienced an alarm condition during the most recent temperature conversion. After every Alarm Search cycle (i.e., Alarm Search command followed by data exchange), the bus master must
return to Step 1 (Initialization) in the transaction sequence. See the *Operation—Alarm Signaling* section for an explanation of alarm flag operation.

SST-DM10 FUNCTION COMMANDS

After the bus master has used a ROM command to address the SST-DM10 with which it wishes to communicate, the master can issue one of the SST-DM10 function commands. These commands allow the master to write to and read from the SST-DM10's scratchpad memory, initiate temperature conversions and determine the power supply mode. The SST-DM10 function commands, which are described below, are summarized in Table in slide 20 and illustrated by the flowchart in slide 22.

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CONVERT T [44h]

This command initiates a single temperature conversion. Following the conversion, the resulting thermal data is stored in the 2-byte temperature register in the scratchpad memory and the SST-DM10 returns to its low-power idle state. If the device is being used in parasite power mode, within 10μs (max) after this command is issued the master must enable a strong pullup on the 1-Wire bus for the duration of the conversion (t_{CONV}) as described in the *Powering the* SST-DM10 section. If the SST-DM10 is powered by an external supply, the master can issue read time slots after the Convert T command and the SST-DM10 will respond by transmitting a 0 while the temperature conversion is in progress and a 1 when the conversion is done. In parasite power mode this notification technique cannot be used since the bus is pulled high by the strong pullup during the conversion.

WRITE SCRATCHPAD [4Eh]

This command allows the master to write at most 5 bytes of data to the SST-DM10's scratchpad. The first data byte is written into the T_H register (byte 2 of the scratchpad), the second byte is written into the T_L register (byte 3), the third byte is written into the configuration register (byte 4) , and the last two bytes are written into the User Bytes 3 and 4. Data must be transmitted least significant bit first. All 5 bytes MUST be written before the master issues a reset, or the data may be corrupted.

READ SCRATCHPAD [BEh]

This command allows the master to read the contents of the scratchpad. The data transfer starts with the least significant bit of byte 0 and continues through the scratchpad until the 9th byte (byte 8 – CRC) is read. The master may issue a reset to terminate reading at any time if only part of the scratchpad data is needed.

COPY SCRATCHPAD 48h]

This command copies the contents of the scratchpad T_H, T_L, configuration registers and User Bytes 3 and 4 (bytes 2, 3, 4, 6 and 7) to EEPROM. If the device is being used in parasite power mode, within 10μs (max) after this command is issued the master must enable a strong pullup on the 1-Wire bus for at least 10ms as described in the *Powering the* SST-DM10 section.

RECALL E^2 B8h]

This command recalls the alarm trigger values (T_H and T_L) , configuration data and User Byte4 and 5 from EEPROM and places the data in bytes 2, 3, 4, 6 and 7, respectively, in the scratchpad memory. The master device can issue read time slots following the Recall E^2 command and the SST-DM10 will indicate the status of the recall by transmitting 0 while the recall is in progress and 1 when the recall is done. The recall operation happens automatically at power-up, so valid data is available in the scratchpad as soon as power is applied to the device.

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READ POWER SUPPLY B4h]

The master device issues this command followed by a read time slot to determine if any SST-DM10s on the bus are using parasite power. During the read time slot, parasite powered SST-DM10s will pull the bus low, and externally powered SST-DM10s will let the bus remain high. See the *Powering the* SST-DM10 section for usage information for this command.

COMMAND	DESCRIPTION	PROTOCOL	1-Wire BUS ACTIVITYAFTER COMMAND IS ISSUED	NOTES
TEMPERATURE CONVERSION COMMANDS				
Convert T	Initiates temperature conversion.	44h	SST-DM10 transmits conversion status to master (not applicable for parasite- powered SST-DM10s).	1
MEMORY COMMANDS				
Read Scratchpad	Reads the entire scratchpad including the CRC byte.	BEh	SST-DM10 transmits up to 9 data bytes to master.	2
Write Scratchpad	Writes data into scratchpad bytes 2, 3, 4, and 6, 7(T_H, T_L, configuration registers and User Bytes).	4Eh	Master transmits 3 or 4 or 5 data bytes to SST-DM10.	3
Copy Scratchpad	Copies T_H, T_L, config register and User Bytes data from the scratchpad to EEPROM.	48h	None	1
Recall E^2	Recalls T_H, T_L, config register and User Bytes data from EEPROM to the scratchpad.	B8h	SST-DM10 transmits recall status to master.	
Read Power Supply	Signals SST-DM10 power supply mode to the master.	B4h	SST-DM10 transmits supply status to master.	

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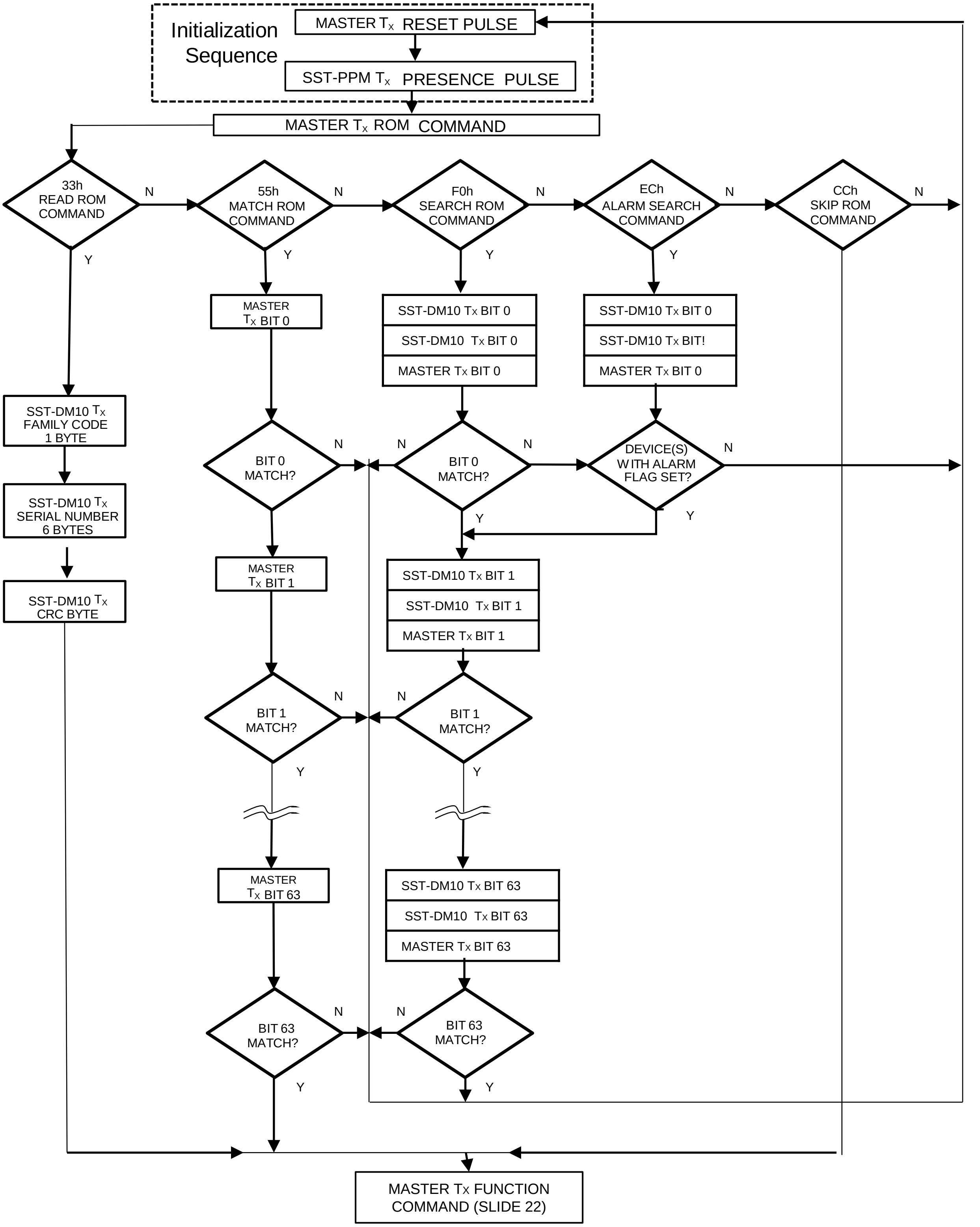

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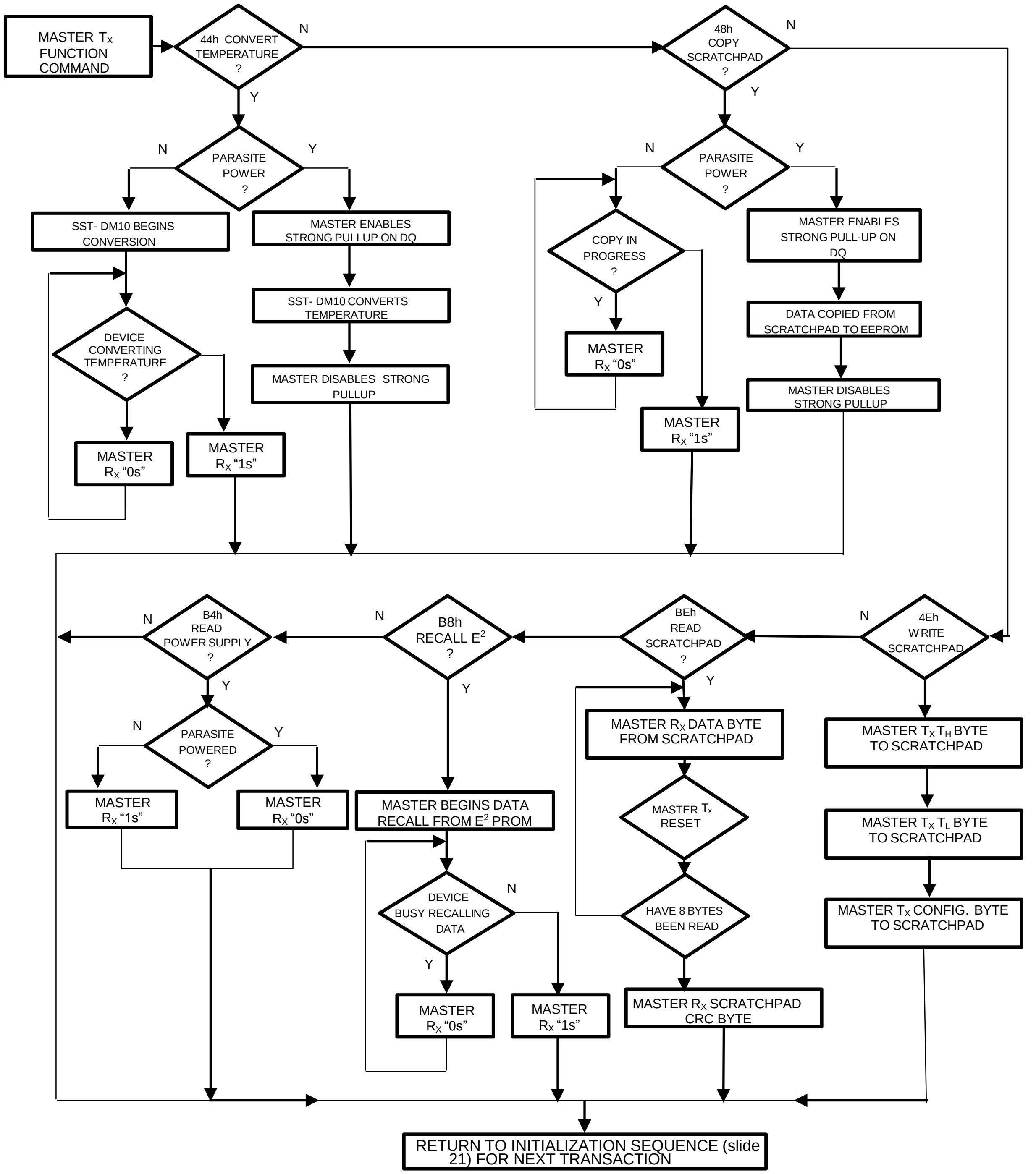

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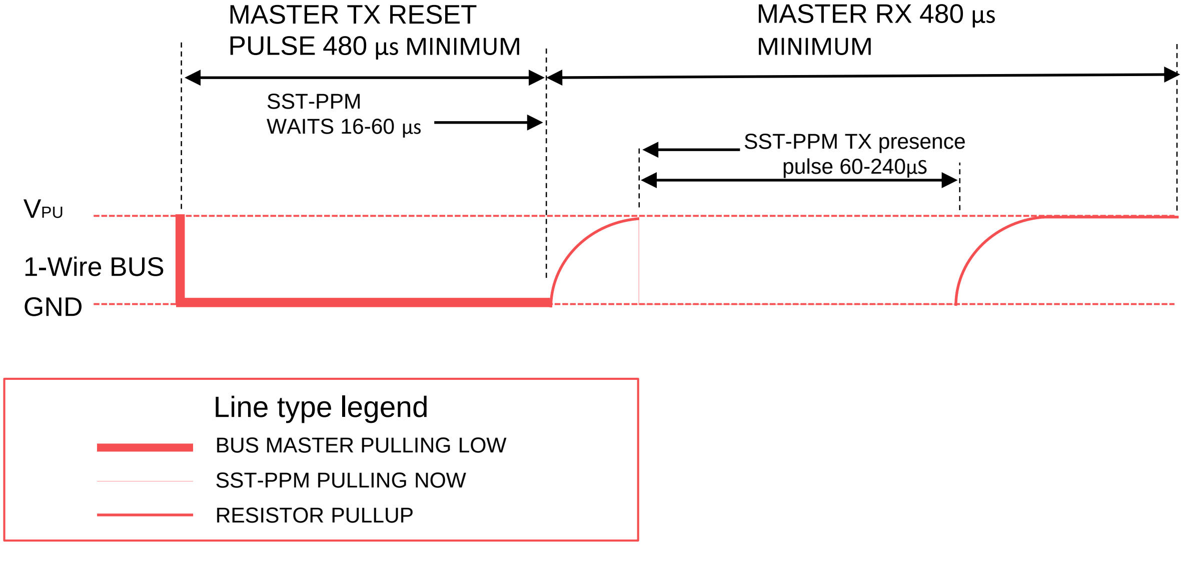
1-WIRE SIGNALING

The SST-DM10 uses a strict 1-Wire communication protocol to ensure data integrity. Several signal types are defined by this protocol: reset pulse, presence pulse, write 0, write 1, read 0, and read 1. The bus master initiates all these signals, with the exception of the presence pulse.

INITIALIZATION PROCEDURE—RESET AND PRESENCE PULSES

All communication with the SST-DM10 begins with an initialization sequence that consists of a reset pulse from the master followed by a presence pulse from the SST-DM10. This is illustrated in Figure below. When the SST-DM10 sends the presence pulse in response to the reset, it is indicating to the master that it is on the bus and ready to operate.

During the initialization sequence the bus master transmits (TX) the reset pulse by pulling the 1-Wire bus low for a minimum of 1ms. The bus master then releases the bus and goes into receive mode (RX). When the bus is released, the 5kΩ pullup resistor pulls the 1-Wire bus high. When the SST-DM10 detects this rising edge, it waits 15µs to 60µs and then transmits a presence pulse by pulling the 1-Wire bus low for 60µs to 240µs.



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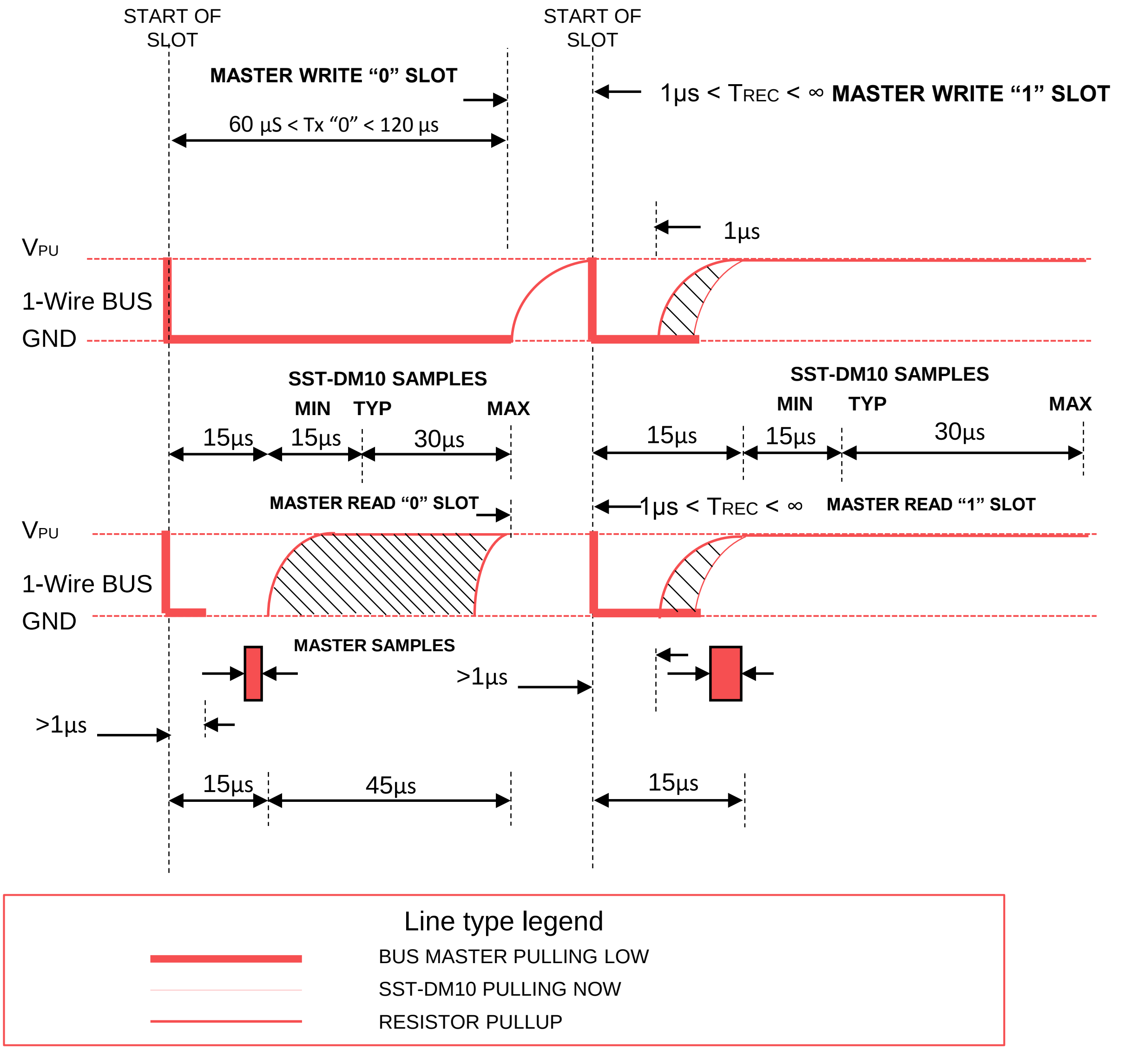

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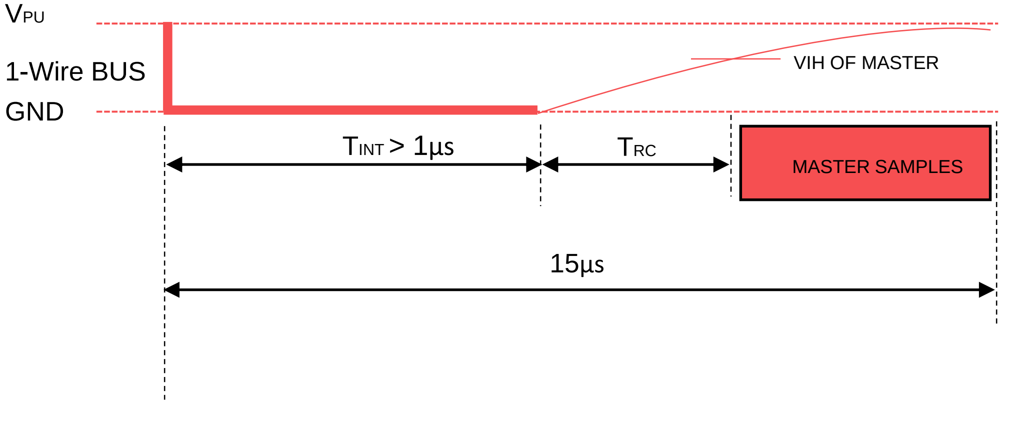
READ TIME SLOTS

The SST-DM10 can only transmit data to the master when the master issues read time slots. Therefore, the master must generate read time slots immediately after issuing a Read Scratchpad [BEh] or Read Power Supply [B4h] command, so that theSST-DM10 can provide the requested data. In addition, the master can generate read time slots after issuing Convert T [44h] or Recall E2 [B8h] commands to find out the status of the operation as explained in the SST-DM10 Function Commands section.

All read time slots must be a minimum of 60µs in duration with a minimum of a 1µs recovery time between slots. A read time slot is initiated by the master device pulling the 1-Wire bus low for a minimum of 1µs and then releasing the bus (see Figure higher). After the master initiates the read time slot, the SST-DM10 will begin transmitting a 1 or 0 on bus. The SST-DM10 transmits a 1 by leaving the bus high and transmits a 0 by pulling the bus low. When transmitting a 0, the SST-DM10 will release the bus by the end of the time slot, and the bus will be pulled back to its high idle state by the pullup resister. Output data from the SST-DM20 is valid for 15µs after the falling edge that initiated the read time slot. Therefore, the master must release the bus and then sample the bus state within 15µs from the start of the slot.

Time diagram below illustrates that the sum of TINIT, TRC, and TSAMPLE must be less than 15µs for a read time slot. time diagram in slide 26 shows that system timing margin is maximized by keeping TINIT and TRC as short as possible and by locating the master sample time during read time slots towards the end of the 15µs period.



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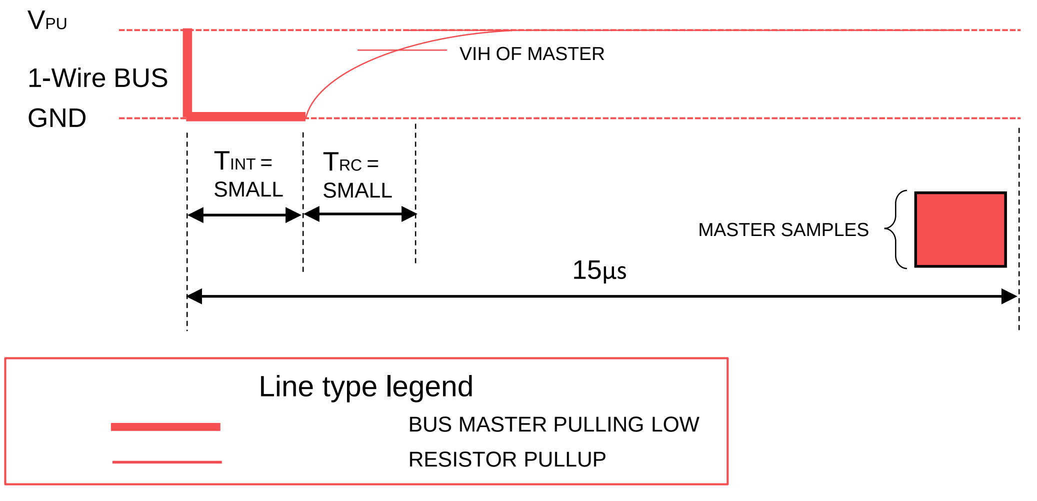

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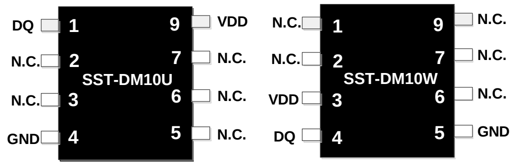
Package variations



MSOP8 SOP8

Pins		Parameters	Definition
MOSP8	SOP8		
2,3,5, 6,7	1,2,6,7,8	N.C.	No Connection
8	3	vDD	Optional V_{DD}. V_{DD} must be grounded for operation in parasite power mode.
1	4	DQ	Data Input/Output. Open-drain 1-Wire interface pin. Also provides power to the device when used in parasite power mode
4	5	GND	Ground

Product	Package	Accuracy
SST-DM10U	MSOP8	±0.5°C
SST-DM10W	SOP8	±0.5°C

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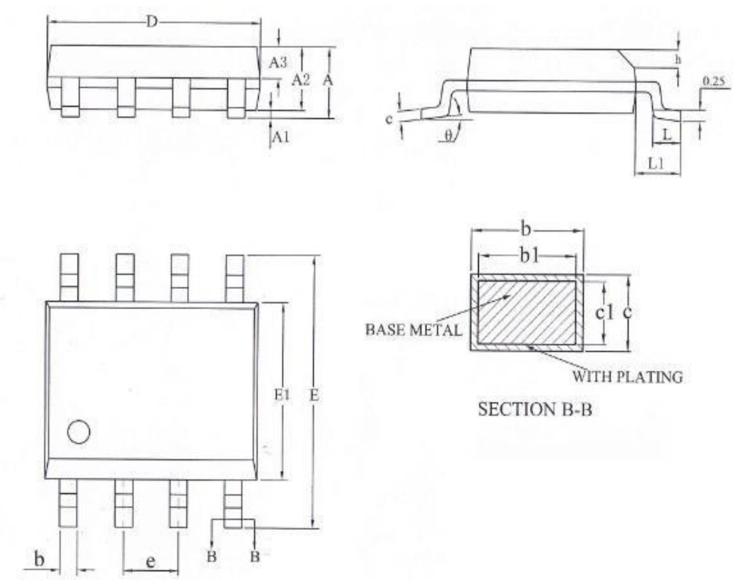
SST-DM10U MSOP8



Symbol	MILLIMETER		
	MIN	NOM	MAX
A	-	-	1.10
A1	0.05	-	0.15
A2	0.75	0.85	0.95
A3	0.30	0.35	0.40
b	0.28	-	0.36
b1	0.27	0.30	0.33
c	0.15	-	0.19
c1	0.14	0.15	0.16
D	2.90	3.00	3.10
E	4.70	4.90	5.10
E1	2.90	3.00	3.10
e	0.65BSC		
L	0.40	-	0.70
L1	0.95REF		
θ	0	-	8°

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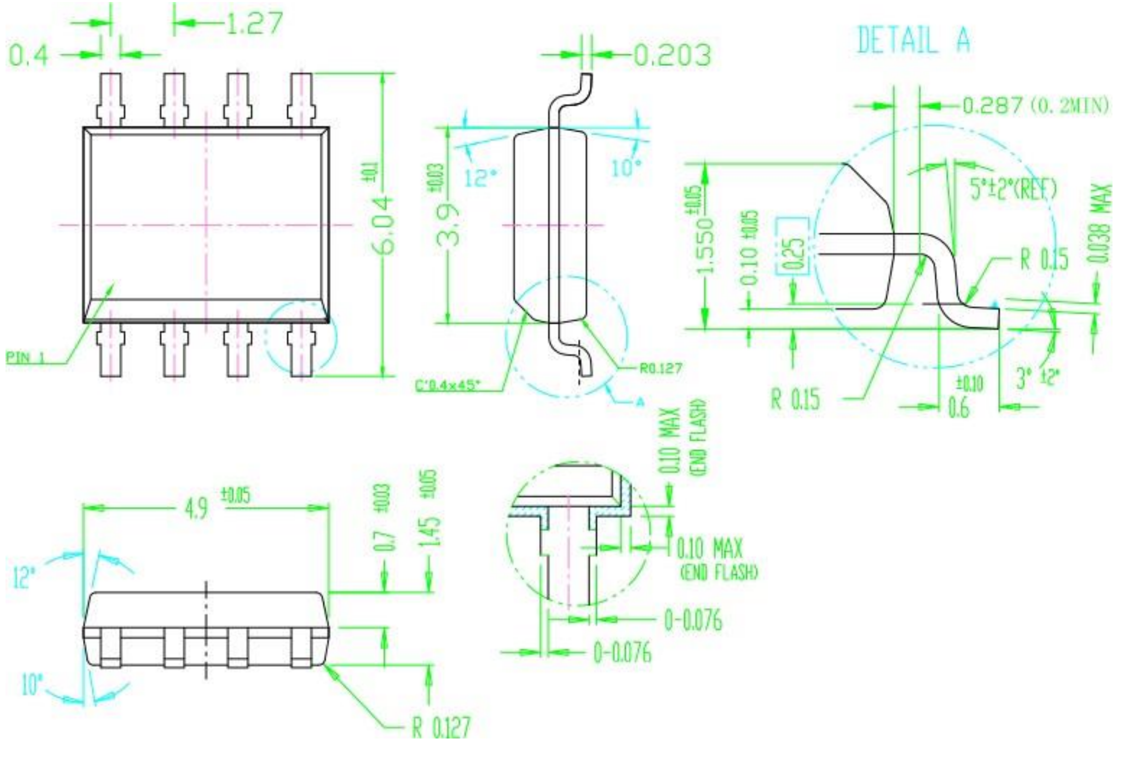

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